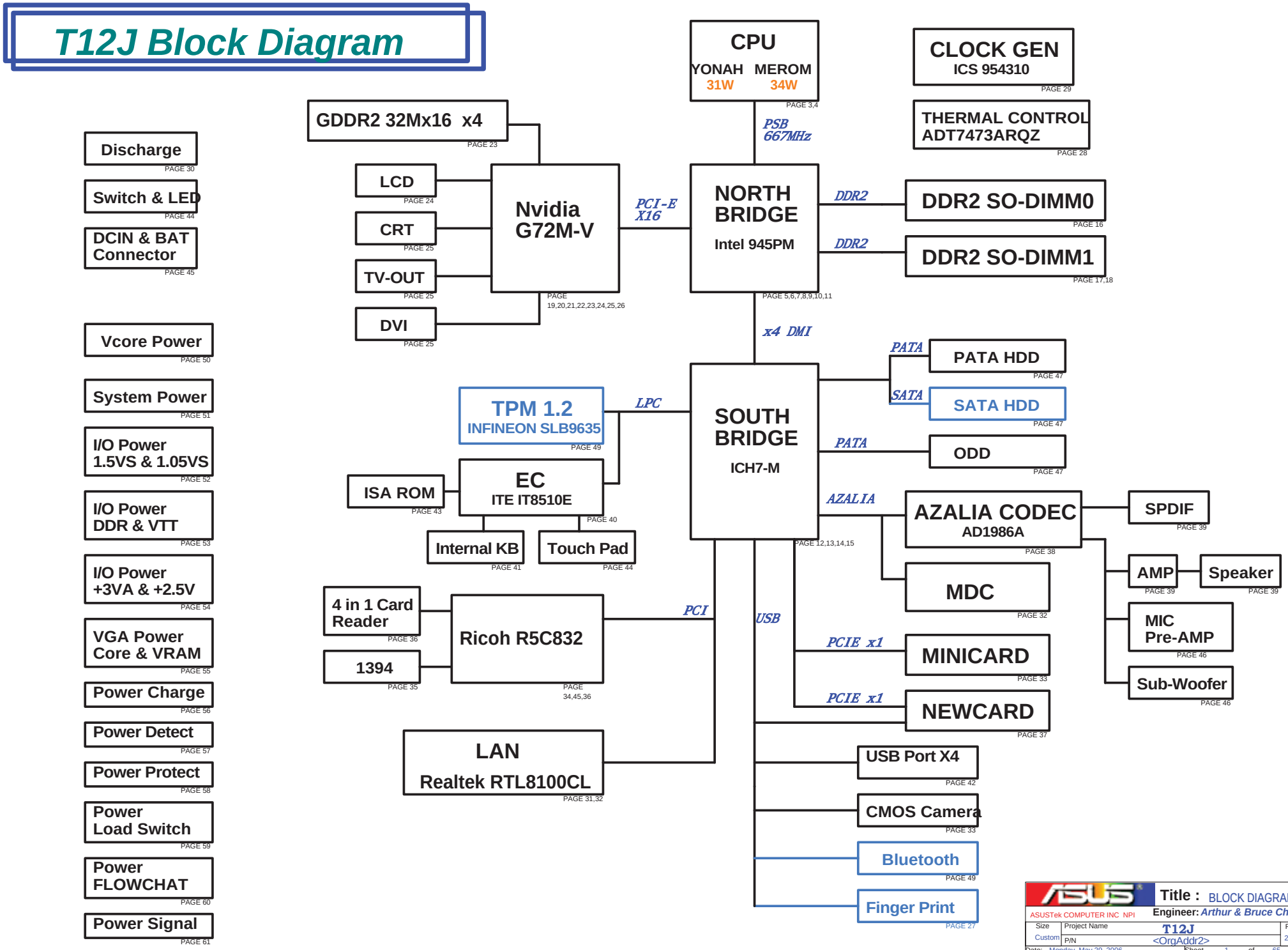
T12J Block Diagram



ASUSTek COMPUTER INC NPI	Title : BLOCK DIAGRAM	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 2.0
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 1 of 65	

EC_ITE8511 GPIO List

Pin	Pin Name	Signal Name	Type	Active
32	PWM0/GPA0	NC		GPO
33	PWM1/GPA1	FAN_PWM	O	High
36	PWM2/GPA2	NC		GPO
37	PWM3/GPA3	NC		GPO
38	PWM4/GPA4	CHG_LED_UP#	O	Low
39	PWM5/GPA5	PWR_LED_UP#	O	Low
40	PWM6/GPA6	BATSEL_3S#	O	Low
43	PWM7/GPA7	LCD_BACKOFF#	O	Low
153	RXD/GPB0	NUM_LED	O	High
154	TXD/GPB1	CAP_LED	O	High
162	GPB2	SCRL_LED	O	High
163	SMCLK0/GPB3	SMB0_CLK	I/0	
164	SMDAT0GPB4	SMB0_DAT	I/0	
5	GA20/GPB5	A20GATE	O	High
6	KBRST#/GPB6	RC_IN#	O	Low
165	GPB7	THRO_CPU	O	High
47	CLKOUT/GPC0	NC		GPO
169	SMCLK1/GPC1	SMB1_CLK	I/0	
170	SMDAT1/GPC2	SMB1_DAT	I/0	
171	GPC3	NC		GPO
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	Low
175	GPC5	OP_SD#	O	Low
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	Low
1	CK32KOUT/GPC7	NC	O	GPO
26	RI1#/WUI0/GPD0	PM_SUSB#	I	Low
29	RI2#/WUI1/GPD1	PM_SUSC#	I	Low
30	LPCRST#/WUI4//GPD2	BUF_PLT_RST#	I	Low
31	ECSCI#/GPD3	EXT_SCI#	O	Low
41	GPD4	NC		GPO
42	GINT/GPD5	NC		GPO
62	TACH0/GPD6	FAN_TACH	I	High
63	TACH1/GPD7	NC	O	GPO
87	ADC4/GPE0	WLAN_SW#	I	Low
88	ADC5/GPE1	NC	I	
89	ADC6/GPE2	MARATHON#	I	Low
90	ADC7/GPE3	DISTP_SW#	I	Low
2	PWRSW/GPE4	PWR_SW#	I	Low
44	WUI5/GPE5	NC		
24	LPCPD#/WUI6/GPE6	LID_EC#	I	Low
25	CLKRUN#/WUI7/GPE7	WLAN_V_ON#	PU	GPO
110	PS2CLK0/GPF0	/	PU	
111	PS2DAT0/GPF1	/	PU	
114	PS2CLK1/GPF2	/	PU	
115	PS2DAT1/GPF3	/	PU	
116	PS2CLK2/GPF4	TP_CLK		
117	PS2DAT2/GPF5	TP_DAT		
118	PS2CLK3/GPF6	PWRLMT#	I	Low
119	PS2DAT3/GPF7	/	PU	
113	FA16/GPG0	FA16		
112	FA17/GPG1	FA17		
104	FA18/GPG2	FA18		
103	FA19/GPG3	NC		
3	FA20/GPG4	THRM_ALERT#	I	
4	FA21/GPG5	NC		
27	LPC80HL/GPG6	PMTHERM#	O	
28	LPC80LL/GPG7	AC_APR_UC#	I	

EC_ITE8511 GPIO List

Pin	Pin Name	Signal Name	Type	Active
48	GPH0	VSUS_ON	O	High
54	GPH1	VSUS_GD#	I	Low
55	GPH2	CPUPWR_GD#	I	Low
69	GPH3	PM_PWRBTN#	O	Low
70	GPH4	SUSC#	O	Low
75	GPH5	SUSB#	O	Low
76	GPH6	CPU_VRON	O	High
105	GPH7	PM_RSMRST#	O	Low
148	GPI0	ICH7_PWROK	O	High
149	GPI1	NC	O	GPO
152	GPI2	NC		GPO
155	GPI3	CHG_EN#	O	Low
156	GPI4	PRECHG	O	High
168	GPI5	BAT_LL#	O	Low
174	GPI6	BAT_LEARN	O	High
148	GPL0	WLAN_ON#	I	Low
149	GPL1	BT_ON#	I	Low
152	GPL2	RF_OFF_SW#	I	Low
155	GPL3	RF_LED_ON	I	High
156	GPL4	NC		GPO
168	GPL5	NC		GPO
174	GPL6	NC		GPO

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Active
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	
C8	GPIO01/REQ5#	PCI_REQ#5	I	
G8	GPIO02/PIRQE#	PCI_INTE#	I	
F7	GPIO03/PIRQF#	PCI_INTF#	I	
F8	GPIO04/PIRQG#	PCI_INTG#	I	
G7	GPIO05/PIRQH#	PCI_INTH#	I	
AC21	GPIO06	BTLED_ON	O	
AC18	GPIO07	NC	I	
E21	GPIO08	EXTSMI#	I	
E20	GPIO09	SATA_DET#0	I	
A20	GPIO10	NC	O	
B23	SMBALERT#/GPIO11	SMB_ALERT#	PU	
F19	GPIO12	KBC_SCI#	I	
E19	GPIO13	NC	O	
R4	GPIO14	NC	O	
E22	GPIO15	WLAN_LED#	O	
AC22	GPIO16	PM_DPRSLPVR	O	
D8	GPIO17/GNT5#	PCI_GNT#5	O	
AC20	GPIO18/STP_PCI#	STP_PCI#	O	
AH18	GPIO19/SATA1GP	NC	PU	
AF21	GPIO20/STP_CPU#	STP_CPU#	O	
AE19	GPIO21/SATA0GP	NC	PU	
A13	GPIO22/REQ4#	PCI_REQ#4	I	
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O	
R3	GPIO24	P4G_LED#	O	
D20	GPIO25	NC	O	
A21	GPIO26/EL_RSVD	BT_DET#	I	
B21	GPIO27/EL_STATE0	NC	I	
E23	GPIO28/EL_STATE1	NC	I	
C3	GPIO29/OC#5	USB_OC#5	I	
A2	GPIO30/OC#6	NEWCARD_OC#	I	
B3	GPIO31/OC#7	USB_OC#7	I	
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	
AC19	GPIO33/AZ_DOCK_EN#	NC	O	
U2	GPIO34/AZ_DOCK_RST#	NC	O	
AD21	GPIO35	NC	O	
AH19	GPIO36/SATA2GP	NC	O	
AE19	GPIO37/SATA3GP	PCB_ID0	I	
AD20	GPIO38	PCB_ID1	I	
AE20	GPIO39	PCB_ID2	I	
A14	GNT4#/GPIO48	PCI_GNT#4	O	
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD17	0	C
1394	AD17	0	B
LAN	AD23		

PCIE Device	Bus		
RTL8111B	PE(T/R)(p/n)1		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
CPU Thermal Sensor(ADT7473)	01011100x (5C)
VGA Thermal Sensor(ADT7473)	0100000x (40)

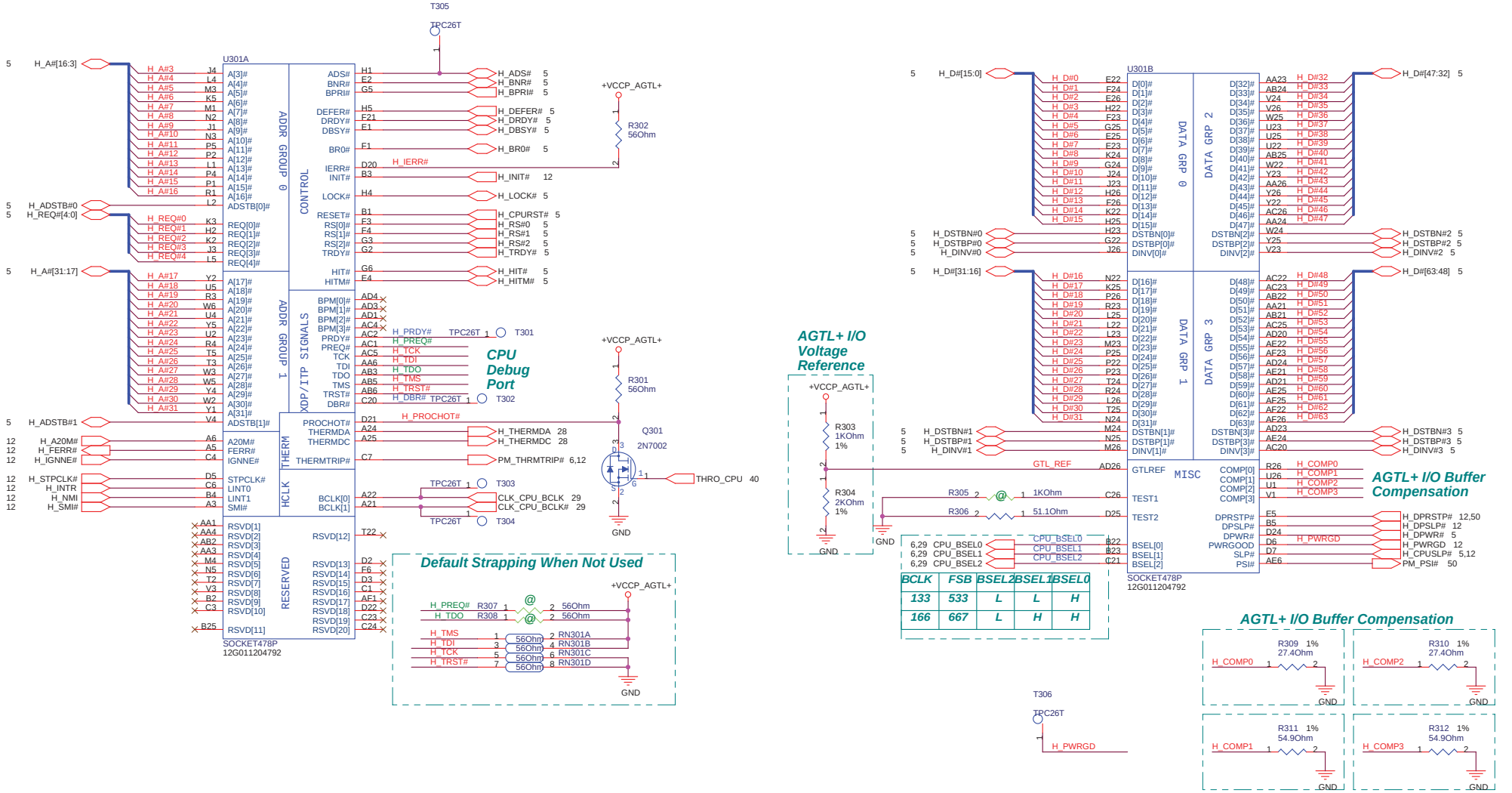
ASUSTek COMPUTER INC NPI

Title : GPIO SETTING

Engineer: Arthur & Bruce Chen

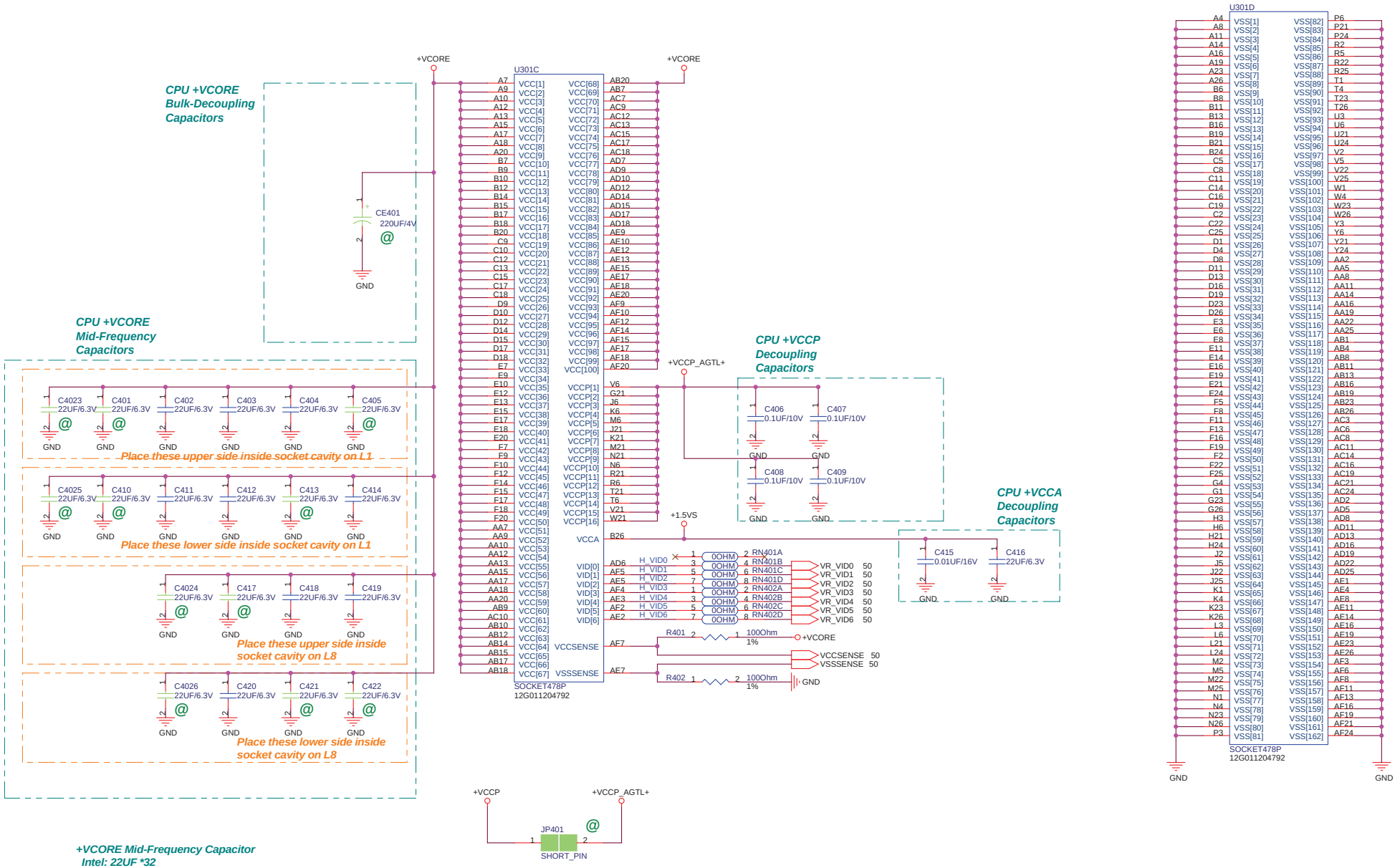
Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 2 of 65

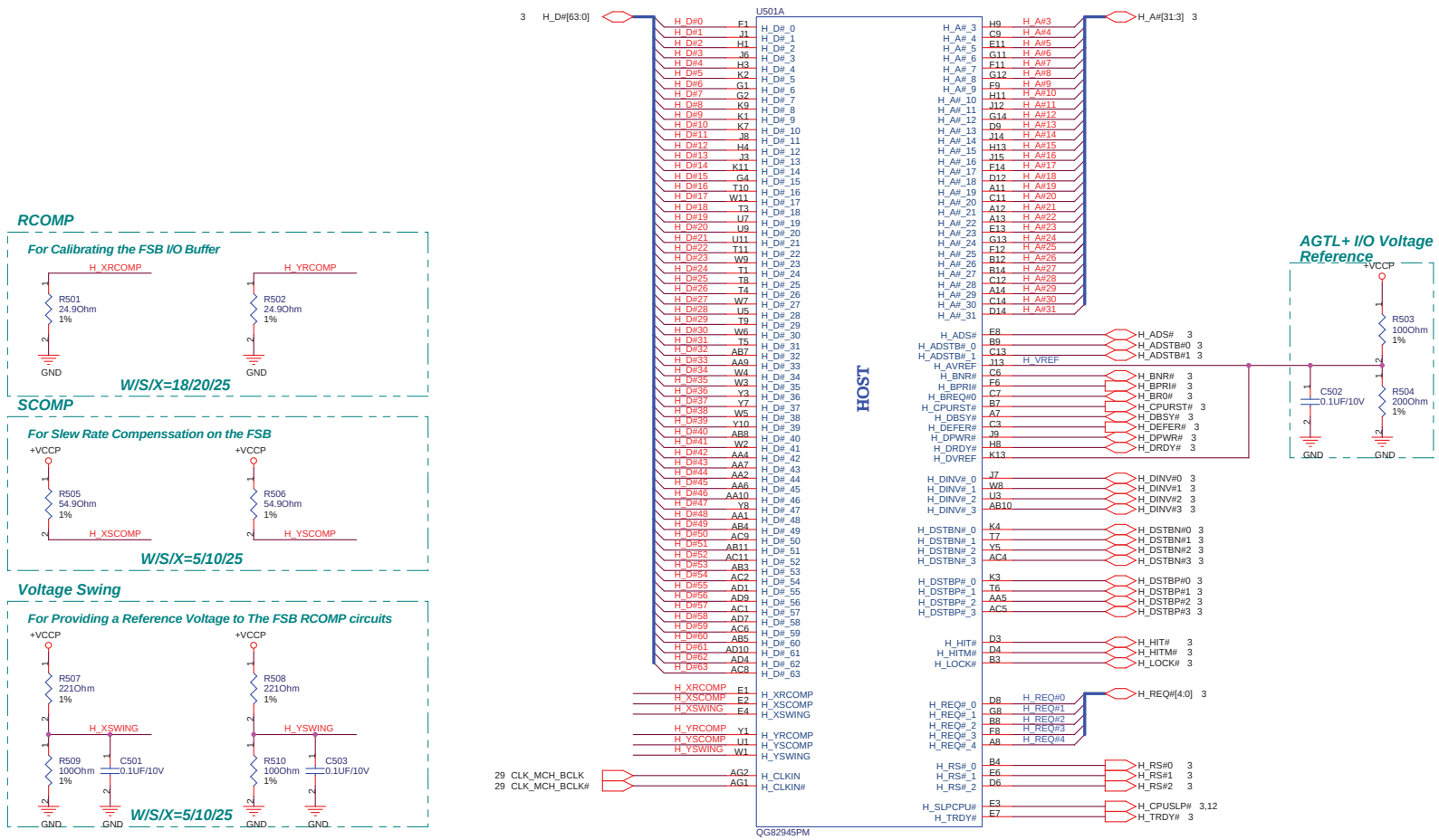


BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Title :	CPU-YONAH(HOST)			
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen			
Size	Project Name	T12J		Rev
Custom	P/N	<OrgAddr2>		1.2
Date: Monday, May 29, 2006	Sheet 3 of 65			



Title : CPU_YONAH(PWR)		
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 4 of 65	



Title :	NB-945PM(HOST)
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen
Size: B / Project Name: T12J	Rev: 0.1
Custom / <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 5 of 65

GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

MCH_CFG_5 — R601 1 — 2 1KOhm @ — GND

CFG[13:12] : GMCH Test Mode

00= Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

CFG7 : CPU Strap

0 = DT/Transpotable CPU
1 = Mobile CPU (D)

MCH_CFG_7 — R602 1 — 2 1KOhm @ — GND

CFG15 : ICH RESET Disable

0 = ICH Reset Disable
1 = Normal Operation (D)

MCH_CFG_15 — R603 1 — 2 1KOhm @ — GND

CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)

MCH_CFG_9 — R606 1 — 2 1KOhm @ — GND

CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)

MCH_CFG_16 — R607 1 — 2 1KOhm @ — GND

CFG10 : HOST PLL VCO Select

0 = Reserved
1 = Mobility (D)

MCH_CFG_10 — R610 1 — 2 1KOhm @ — GND

CFG18 : VCC Select

0 = 1.05V (D)
1 = 1.5V

+3VS — MCH_CFG_18 — R611 1 — 2 1KOhm @ — GND

CFG11 : PSB 4x CLK Enable

0 = 4x Enable
1 = 8x Enable (D)

MCH_CFG_11 — R613 1 — 2 1KOhm @ — GND

CFG19 : DMI Lane Reversal

0 = Normal Operation (D)
1 = Lanes Reversed

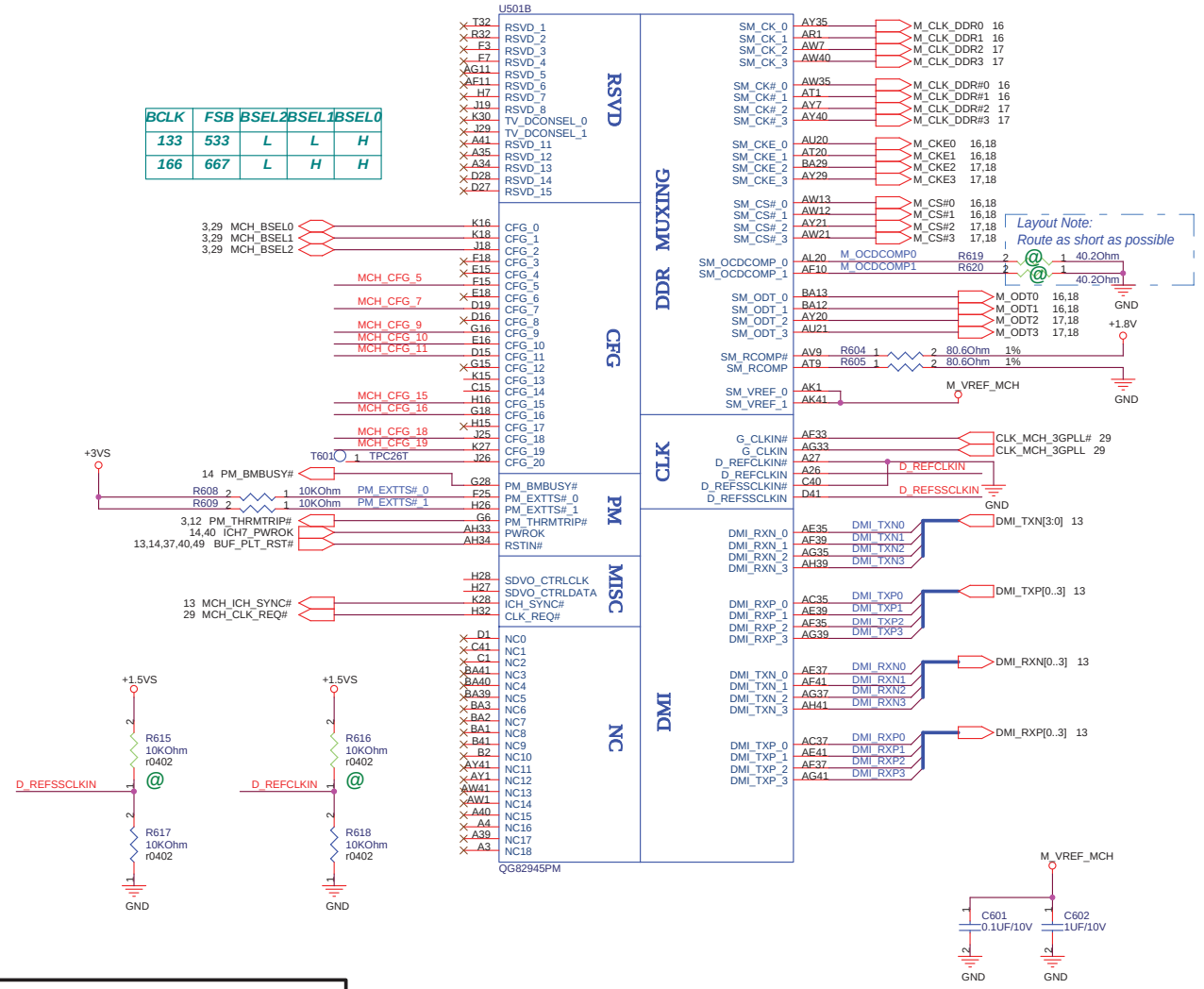
+3VS — MCH_CFG_19 — R614 1 — 2 1KOhm @ — GND

Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

CFG All are sampled with respect to the leading edge of the GMCH PWROK

2:0	FSB Freq select	001 = FSB533 011 = FSB667
4:3		
5	DMI X 2 Select	0 = DMI X 2 1 = DMI X 4
6		(Default)
7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
8		
9	PCIE Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal (Default)
11:10		
13:12	XOR/ALLZ	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal operation (Default)
15:14		
16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
17		
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
18	VCC select	0 = 1.05V (Default) 1 = 1.5V
19	DMI Lane Reversal	0 = Normal (Default) 1 = Reverse Lanes
20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operational(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.
SDVOCRTL_DATA has internal pulldown resistors.

ASUSTek COMPUTER INC NPI

Title : NB-945PM(DMI & CFG)

Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

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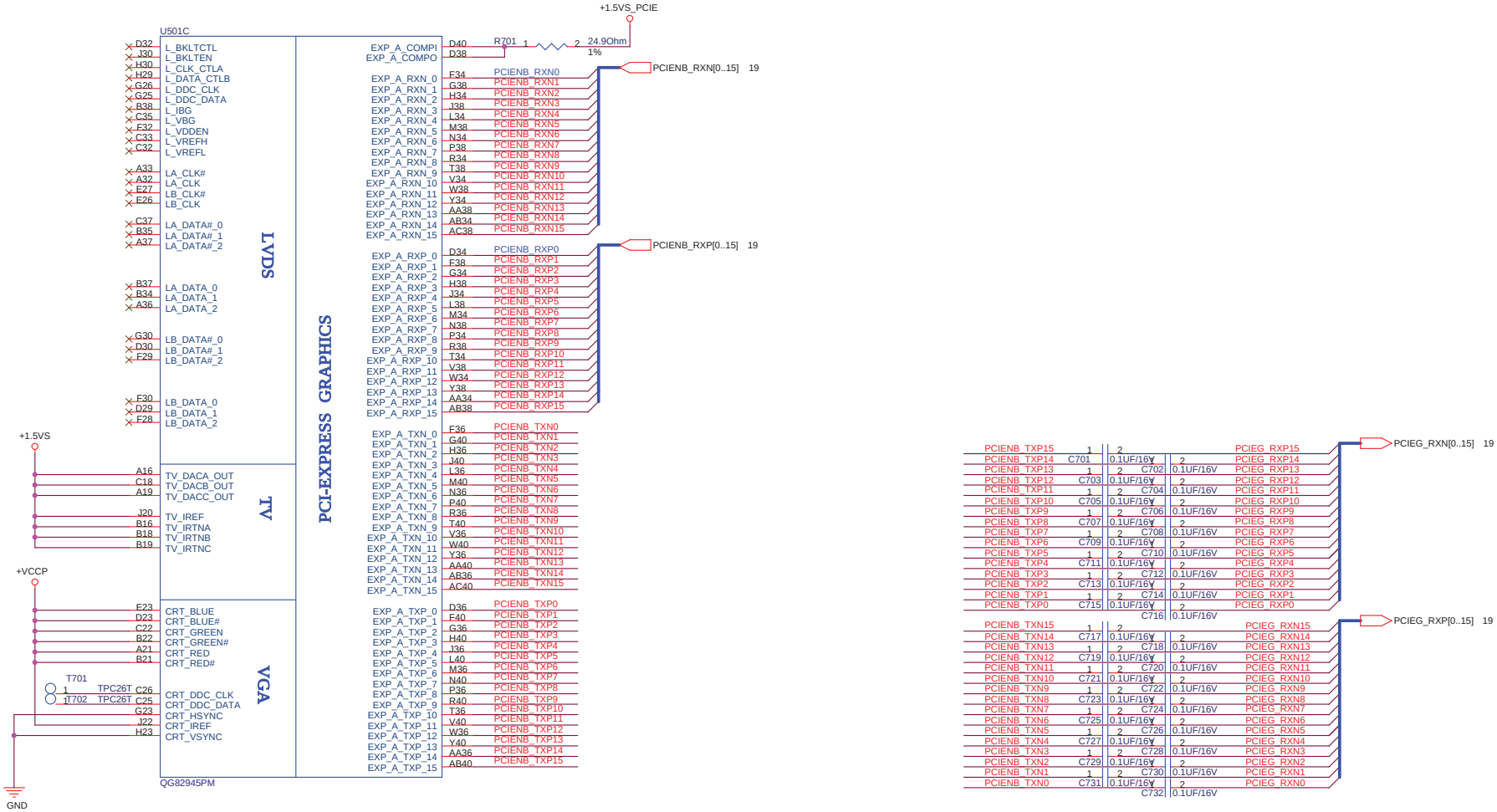
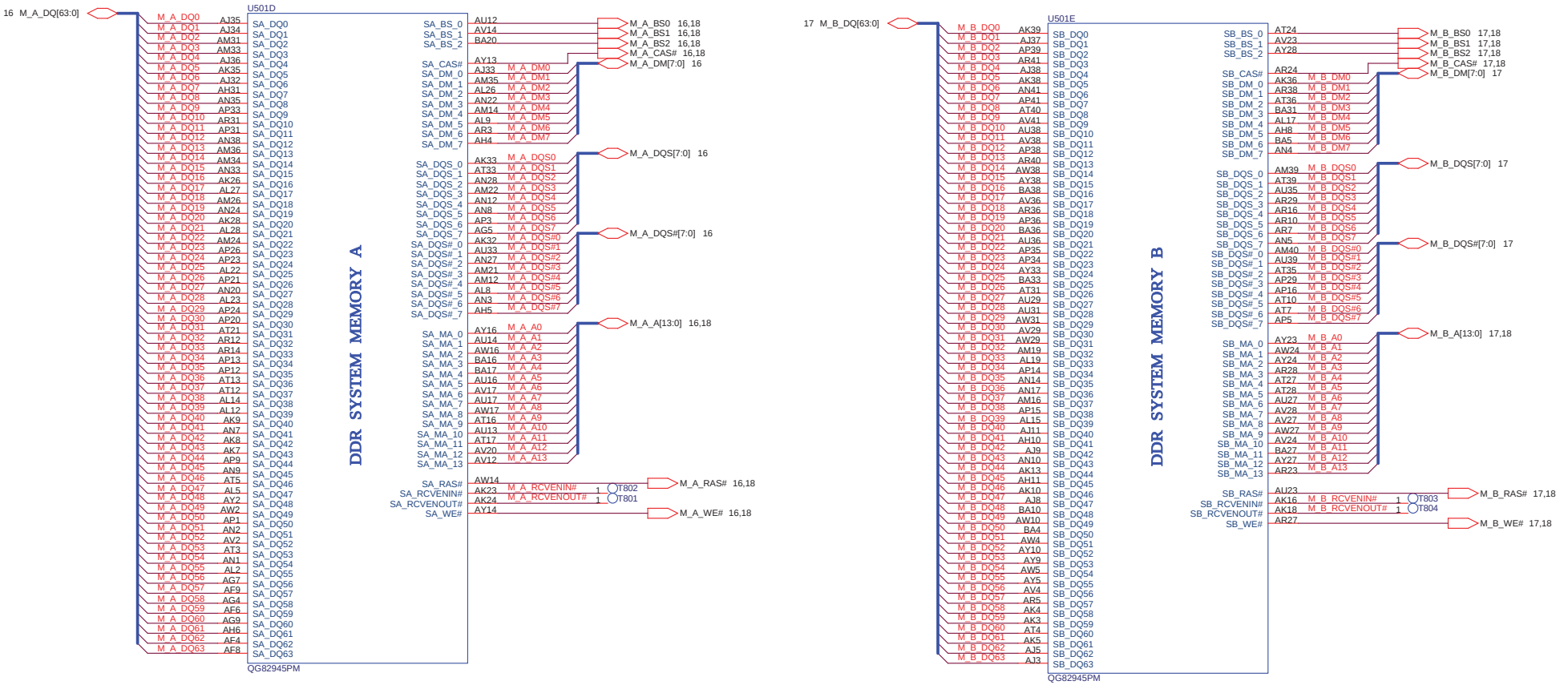
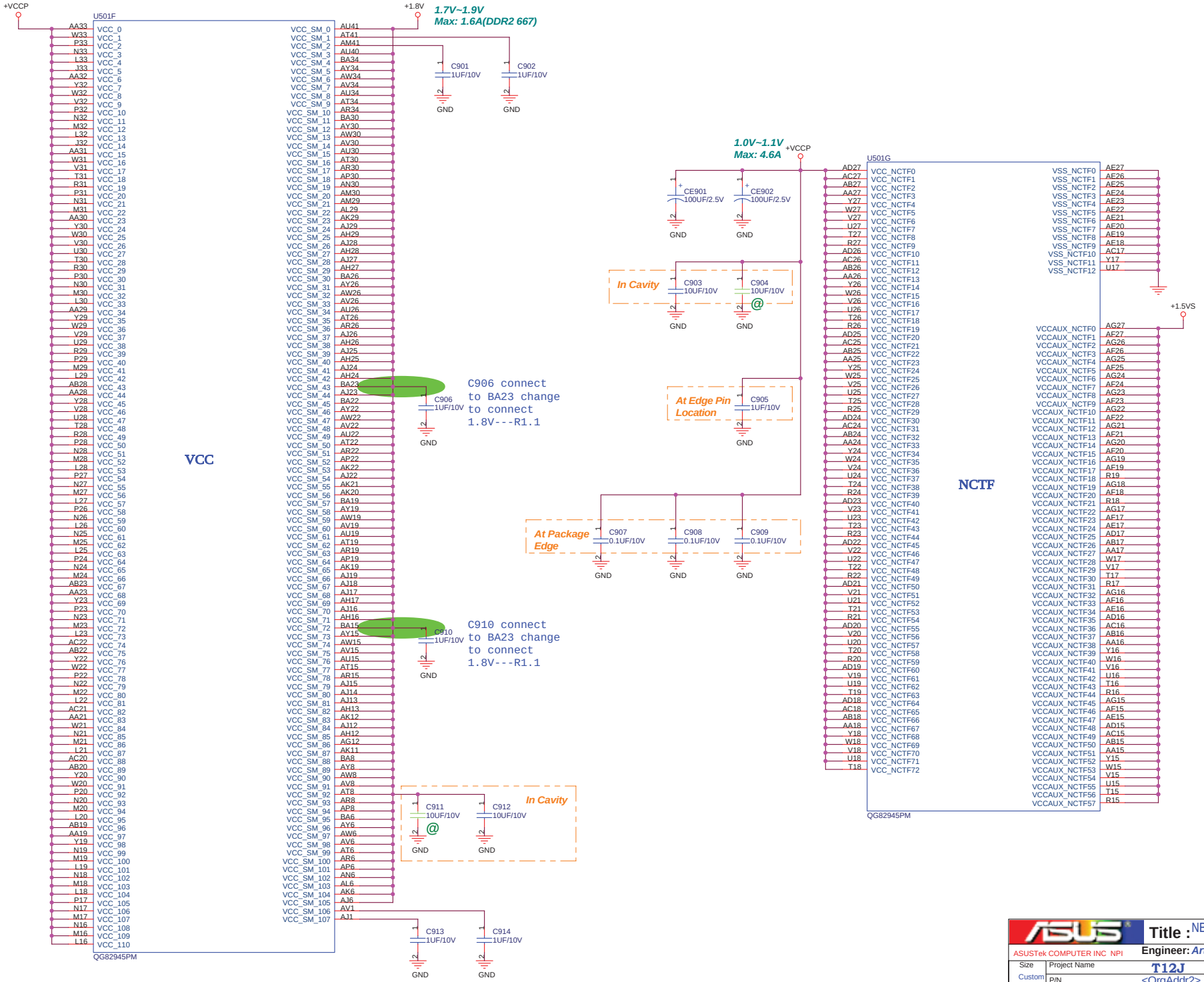


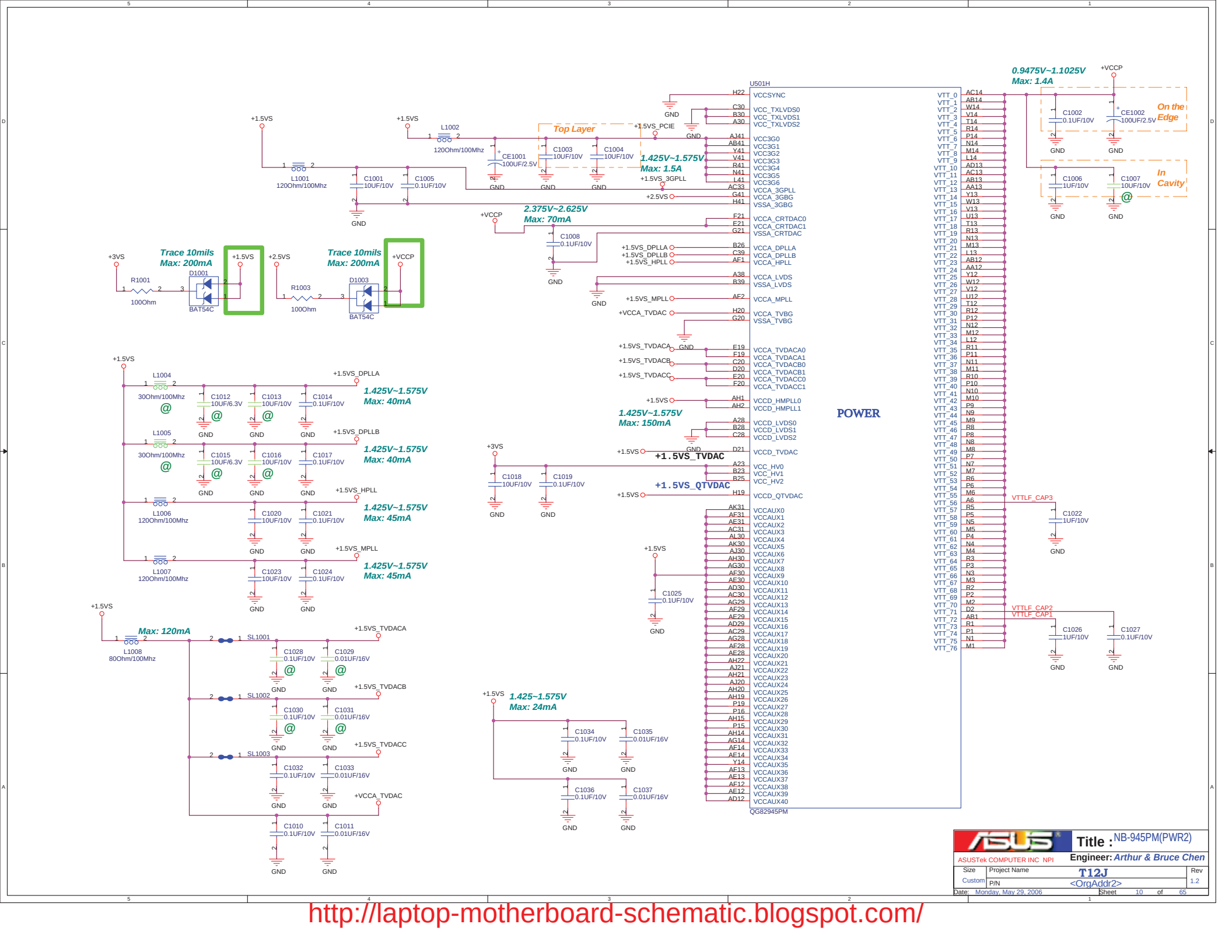
Title :	NB_945PM(GRAPHIC)
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen
Size: Custom	Project Name: T12J
P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 7 of 65

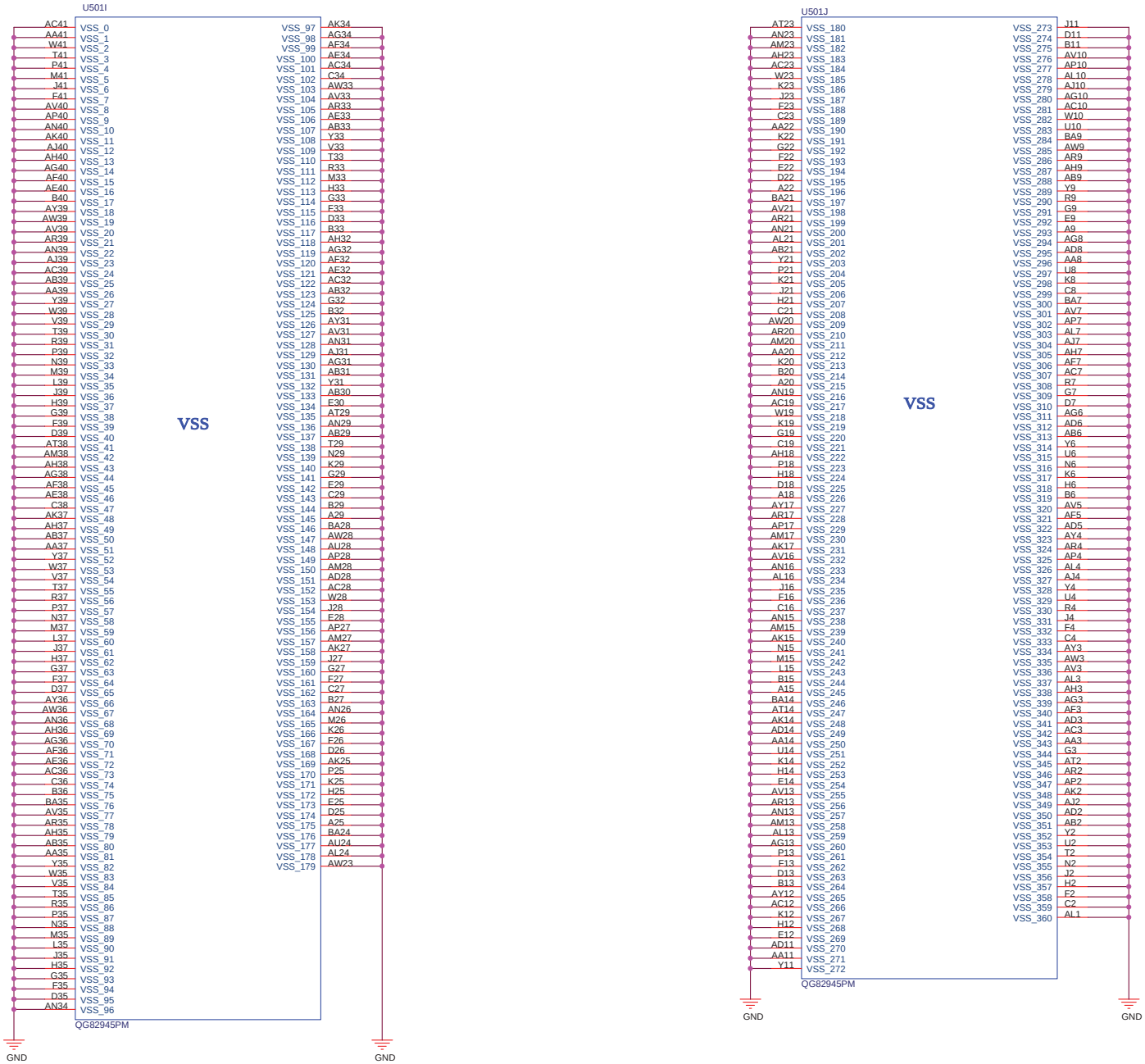


ASUSTek COMPUTER INC NPI	Title : NB-945PM(DDR2)		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 8 of 65		



Title : NB-945PM(PWR)		
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 9 of 65	





ASUSTek COMPUTER INC NPI	Title : NB-945PM(GND)		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 1.2
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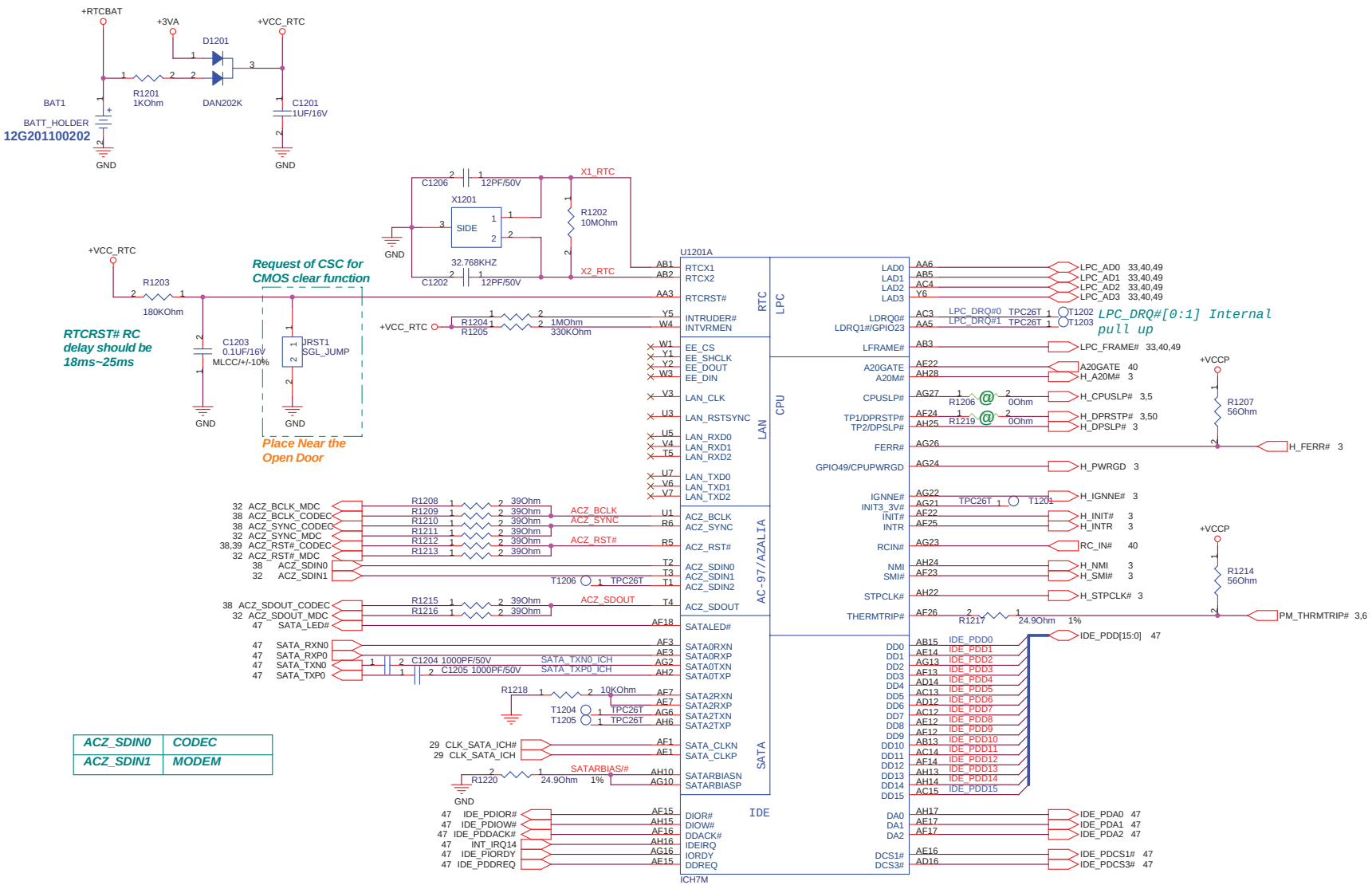

ASUSTek COMPUTER INC NPI

Title : SB-ICH7-M(1)

Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

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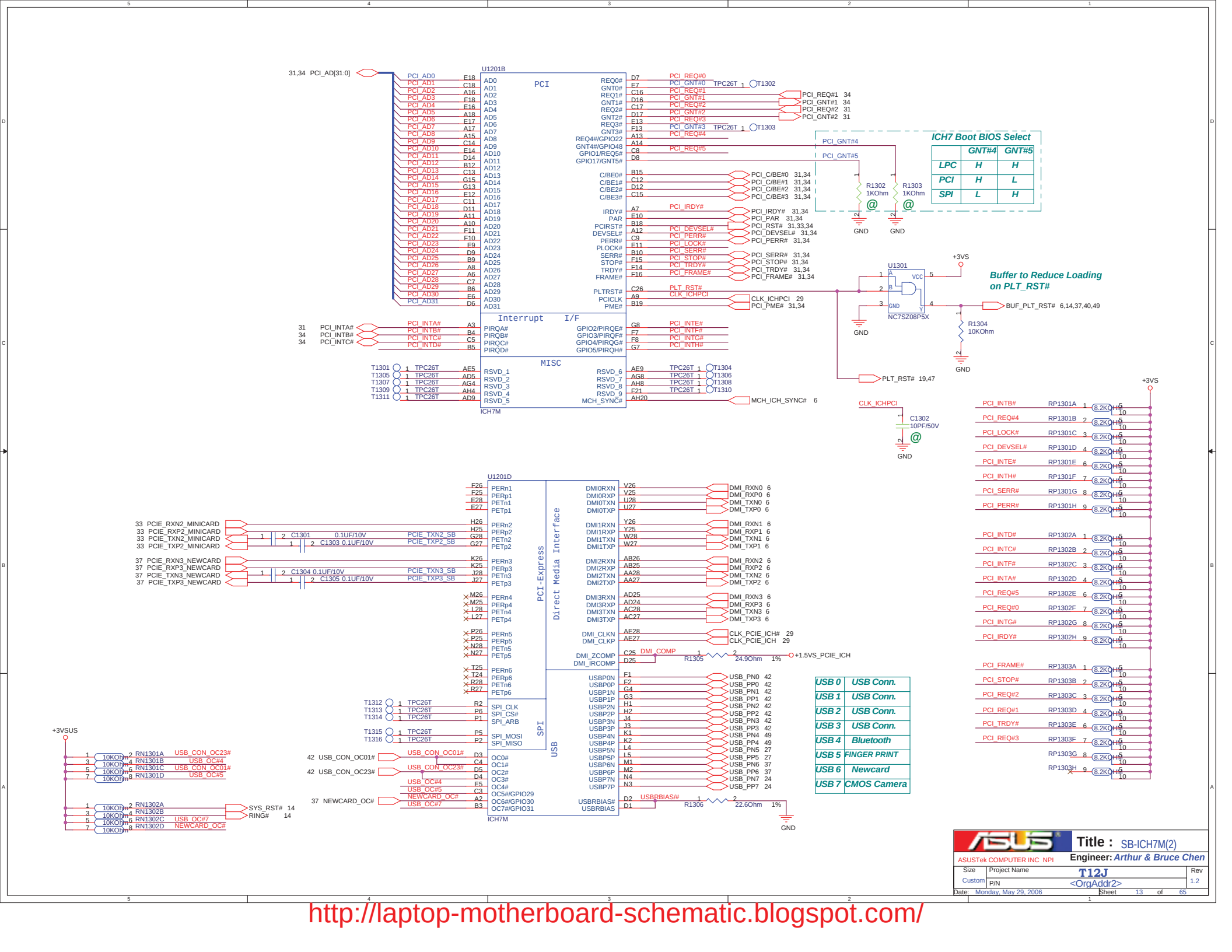
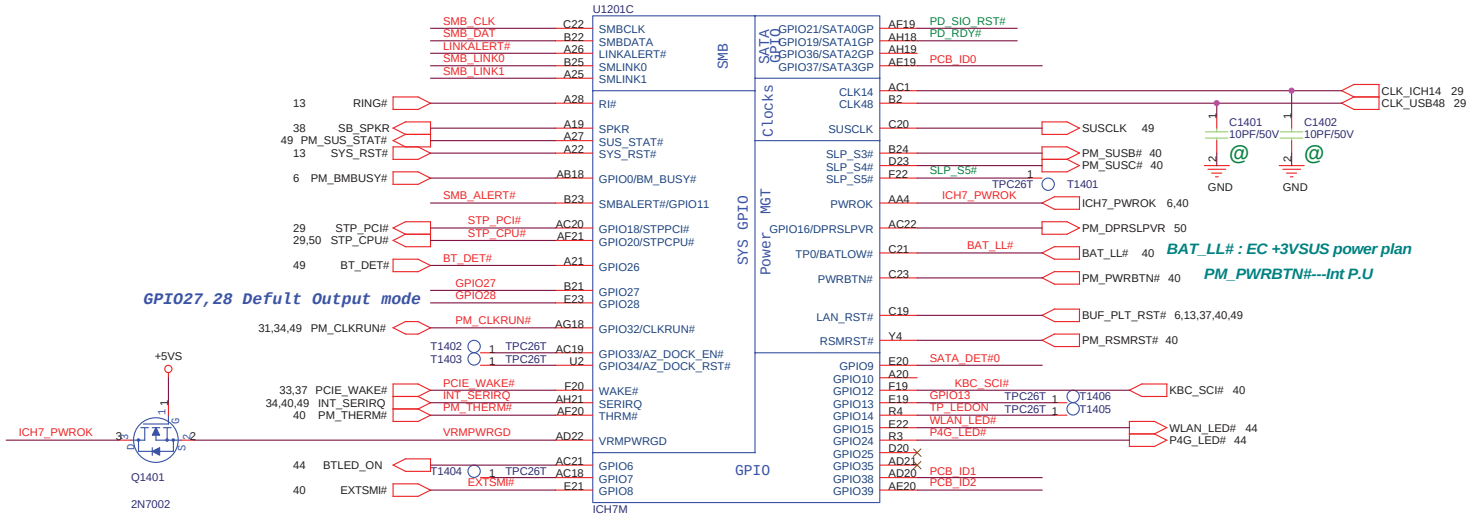
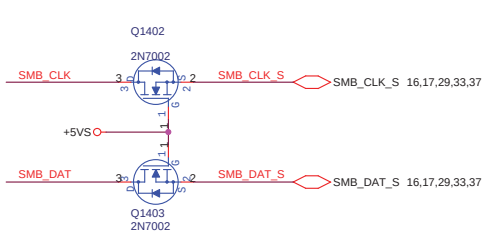
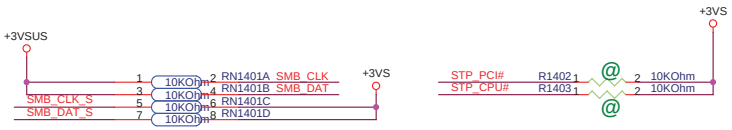
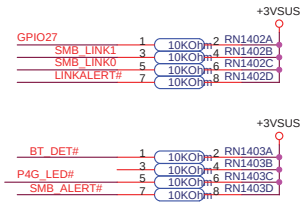
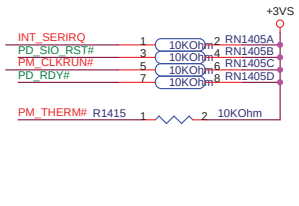


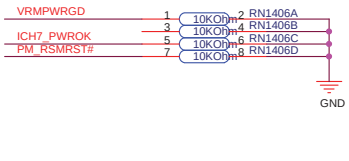


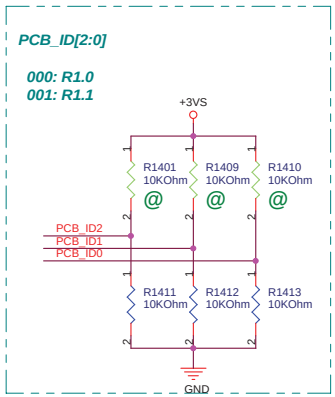




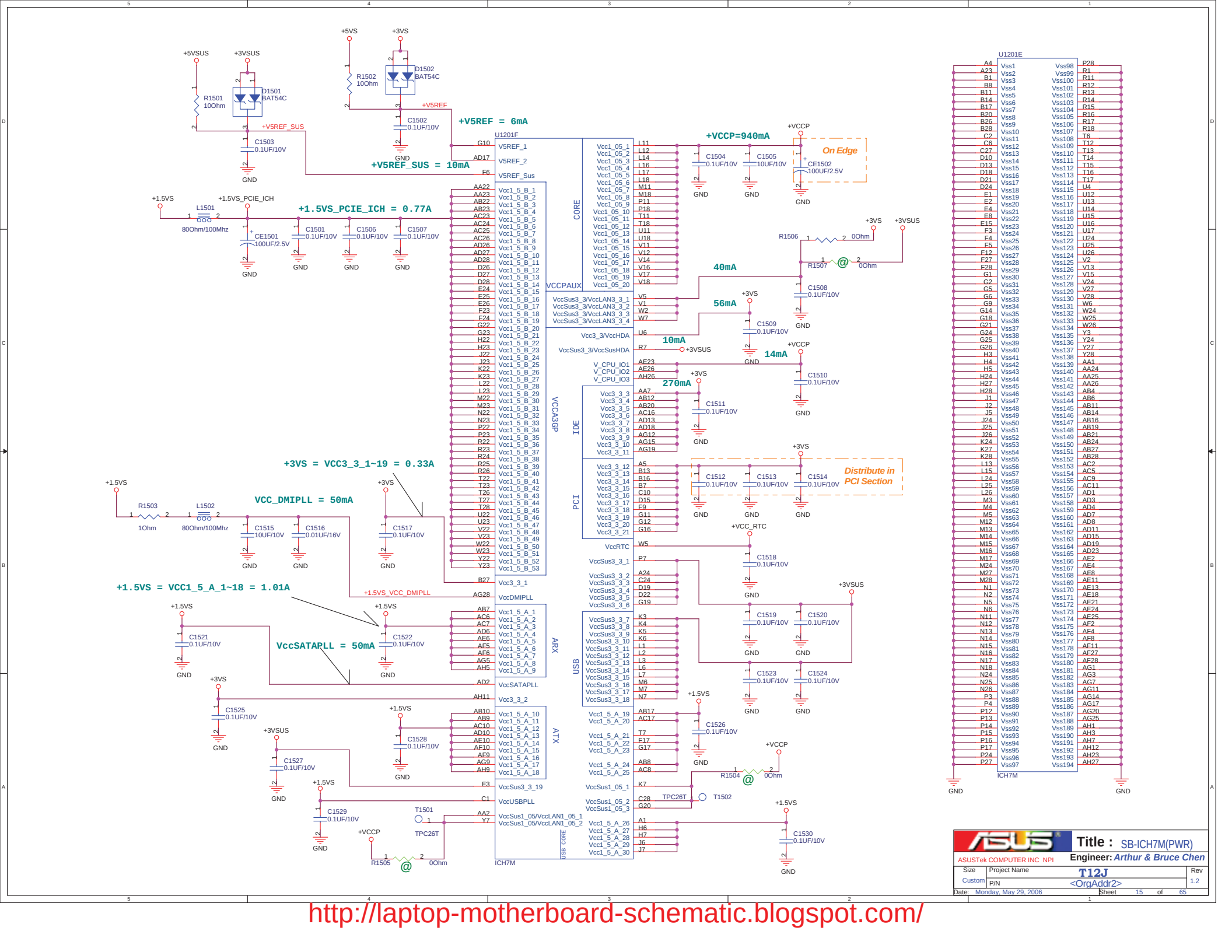


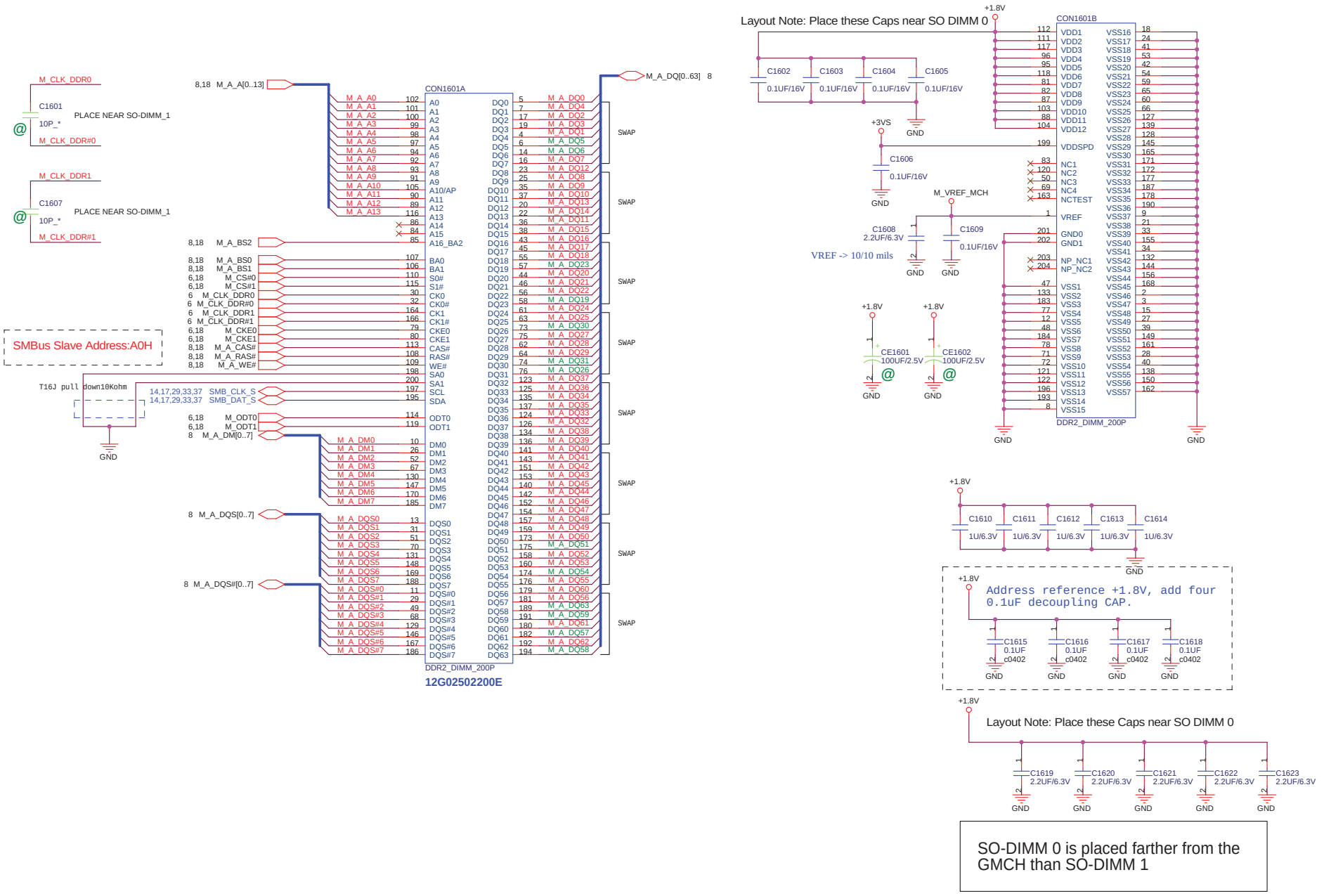






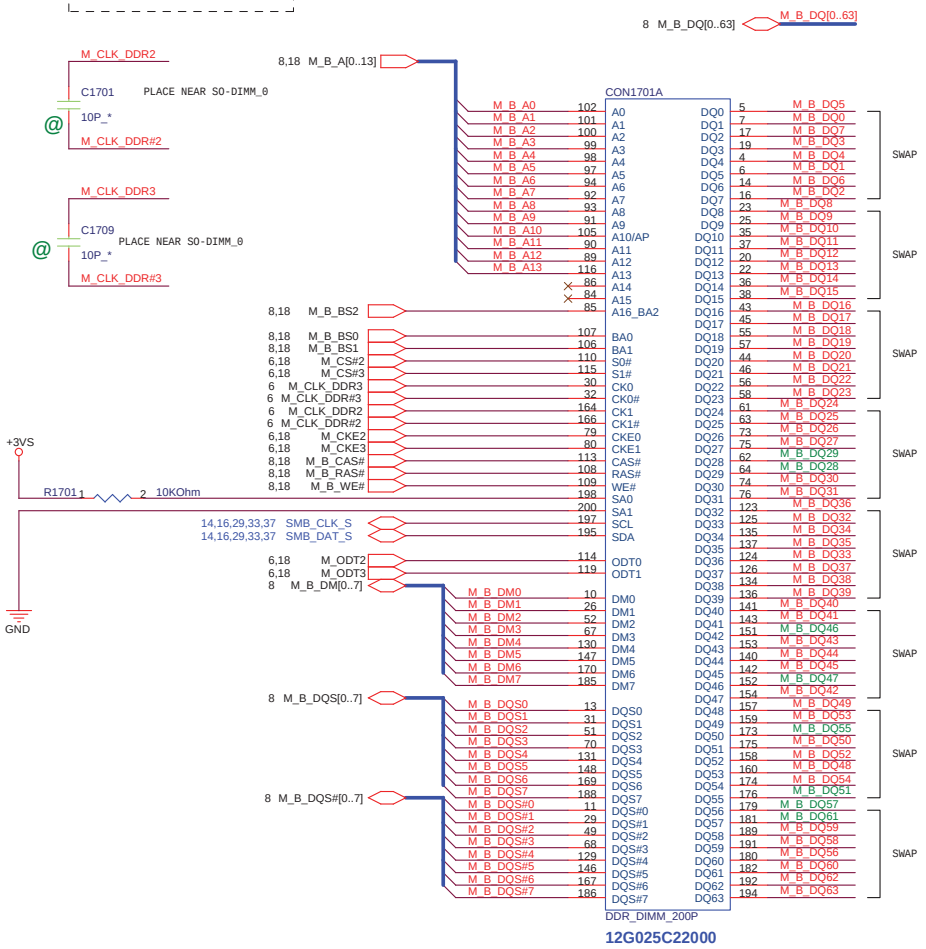
ASUSTek COMPUTER INC NPI	Title : SB-ICH7M(3)		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 14 of 65		



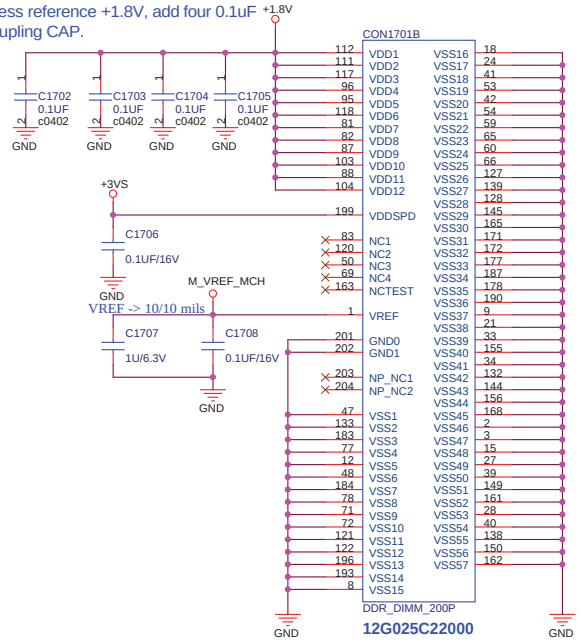


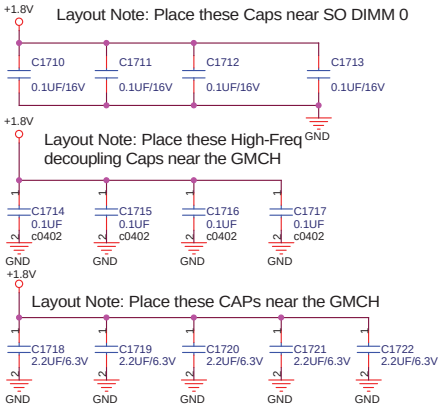
ASUSTek COMPUTER INC NPI	Title : DDR2 SO-DIMM0	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 16 of 65	

SMBus Slave Address:A4H

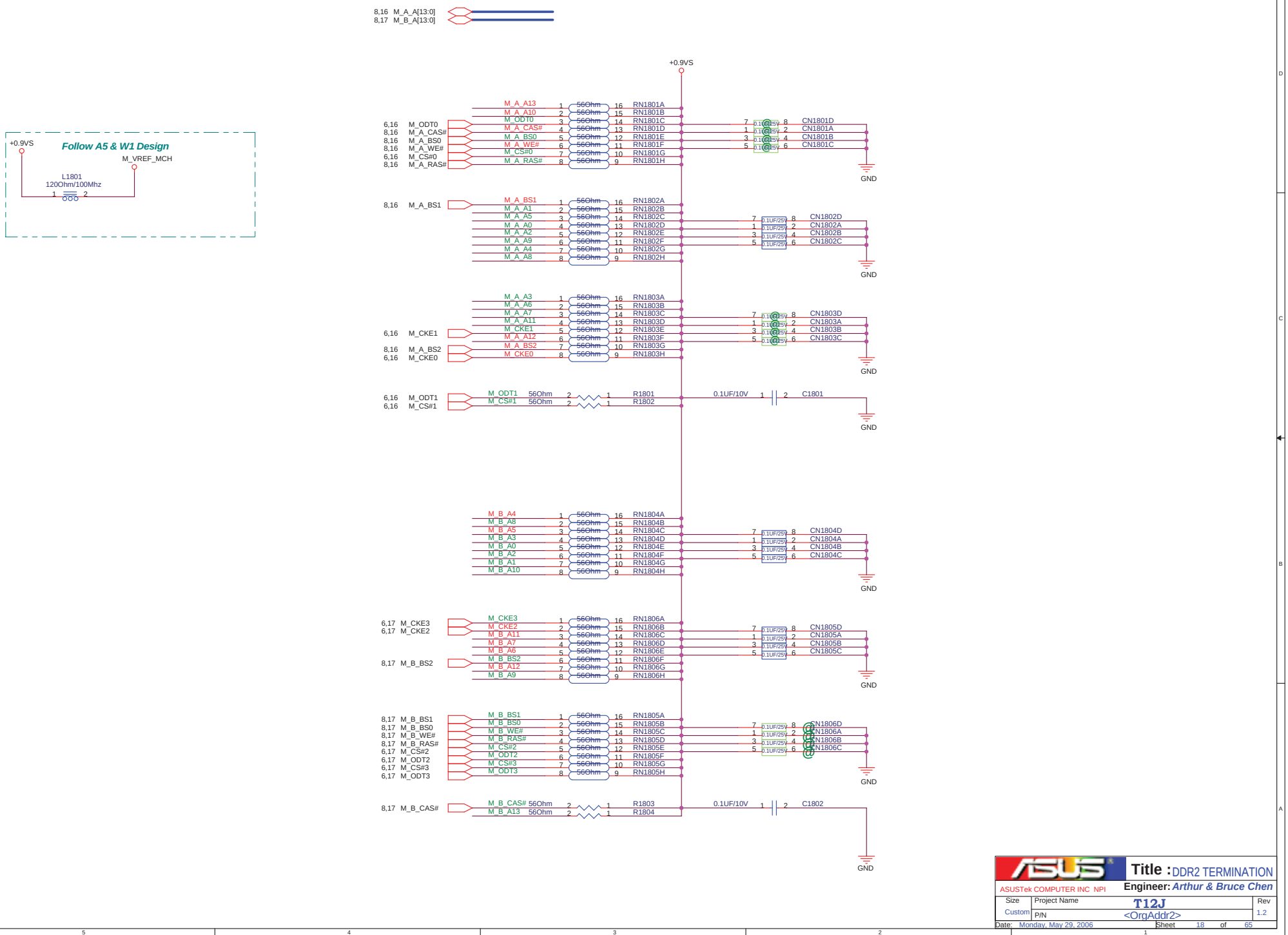


Address reference +1.8V, add four 0.1uF decoupling CAP.

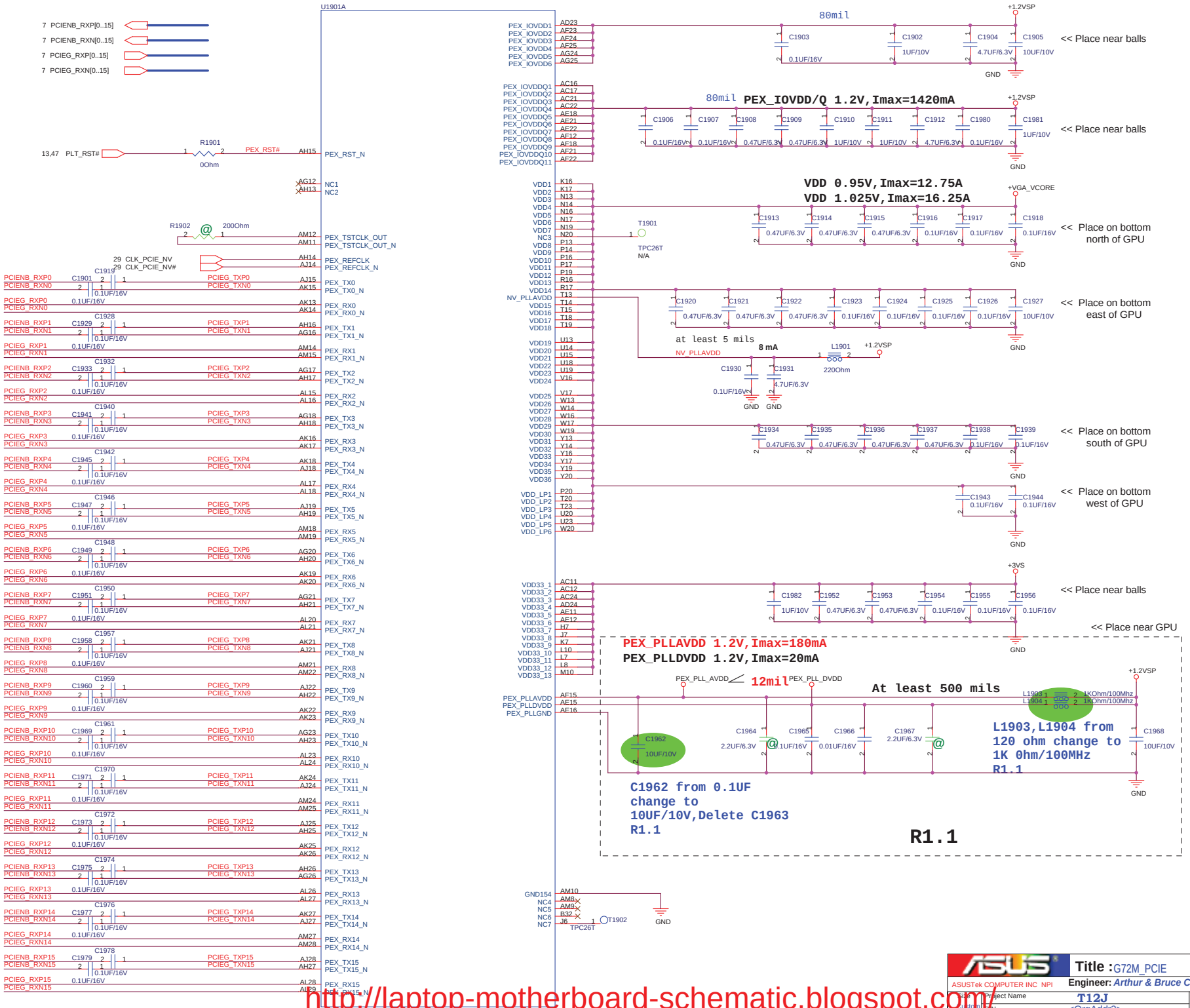


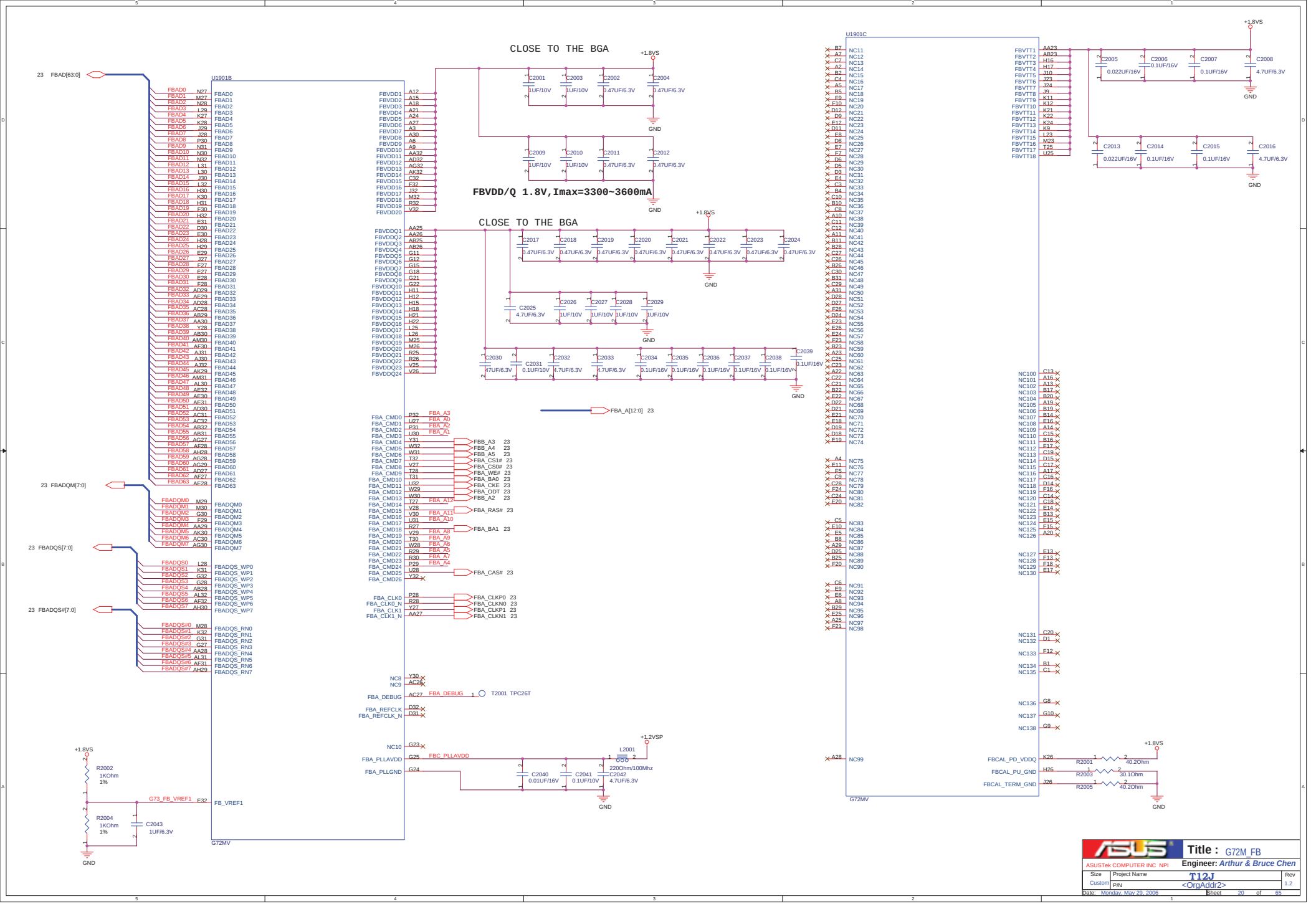


ASUSTek COMPUTER INC NPI	Title : DDR2 SO-DIMM1	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 17 of 65	



ASUSTek COMPUTER INC NPI	Title : DDR2 TERMINATION		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 18 of 65		





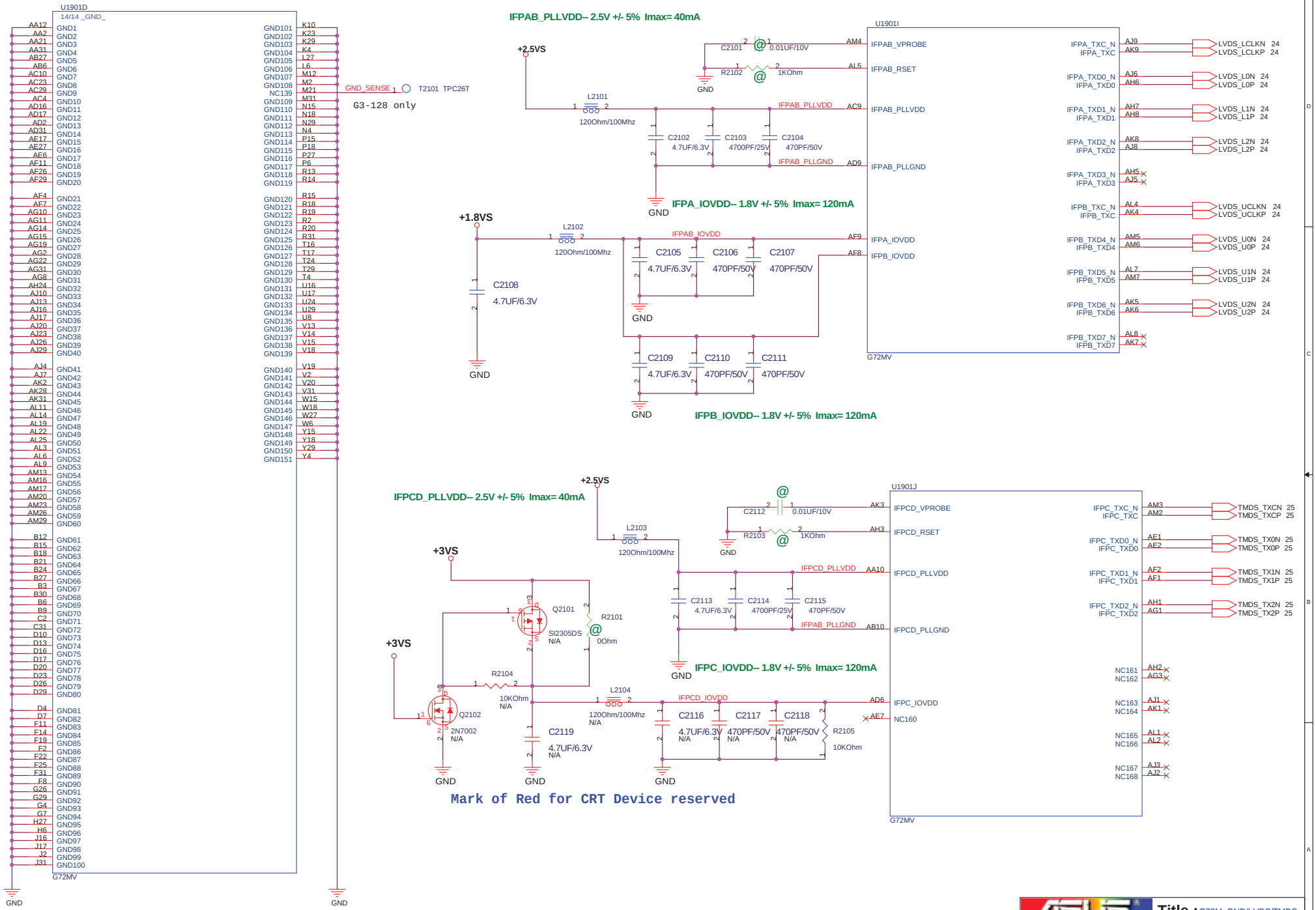
ASUSTek COMPUTER INC NPI

Title : G72M_FB

Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 20 of 65



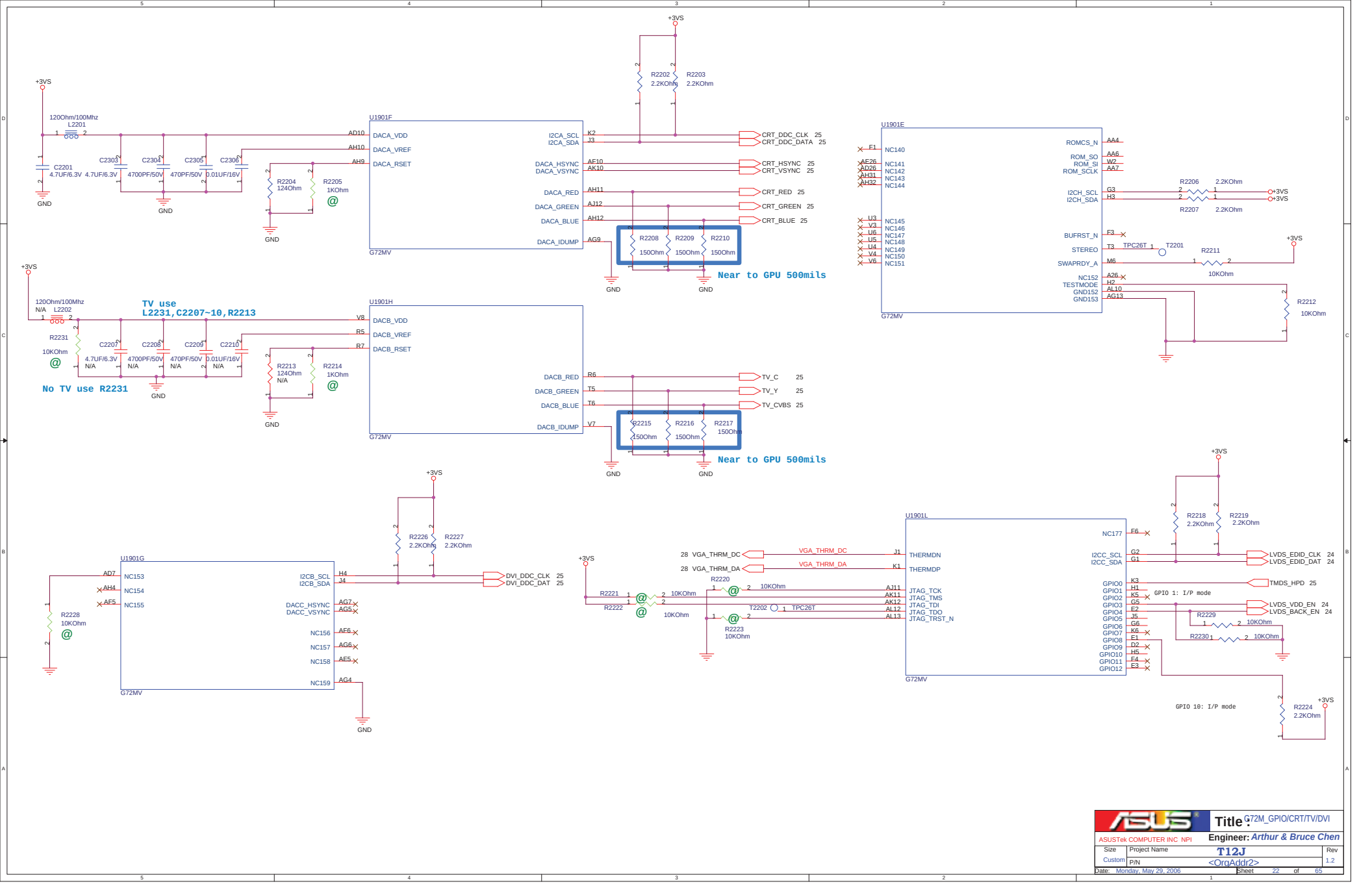
Title : G72M_GND/LVDS/TMDS

ASUSTek COMPUTER INC NPI

Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

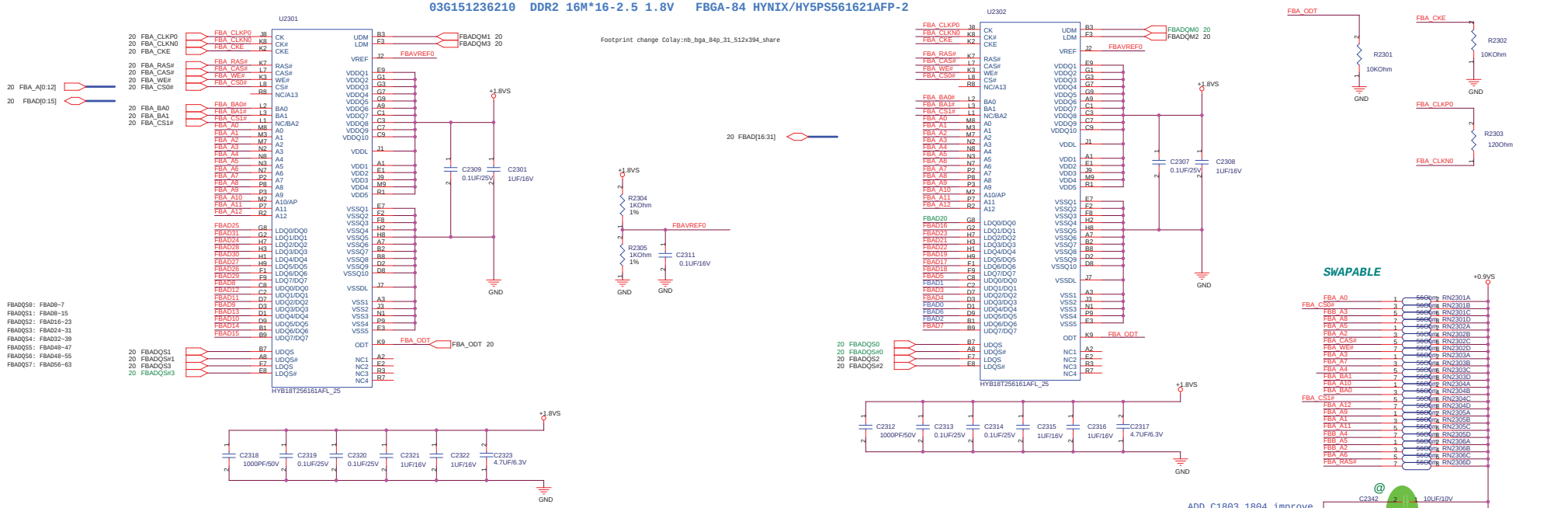
Date: Monday, May 29, 2006 Sheet 21 of 65



ASUSTek COMPUTER INC NPI	Title: G72M_GPIO/CRT/TV/DVI	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 22 of 65	

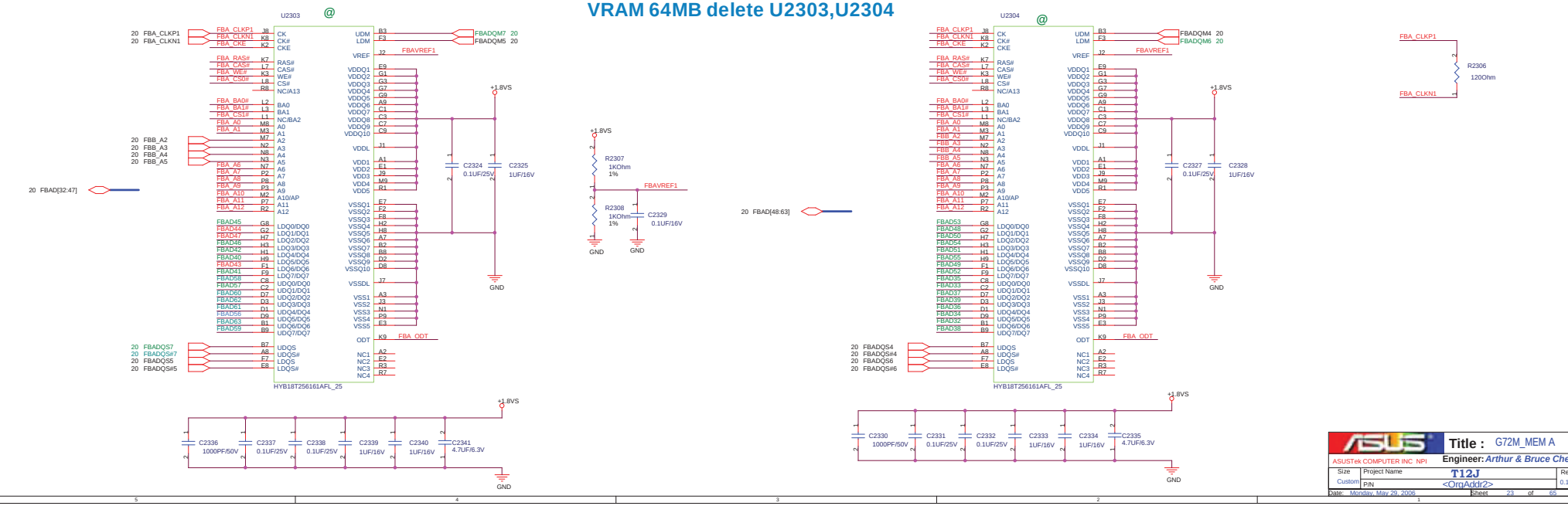
Partition A Low 32 bits

03G151236210 DDR2 16M*16-2.5 1.8V FBGA-84 HYNIX/HY5PS561621AFP-2

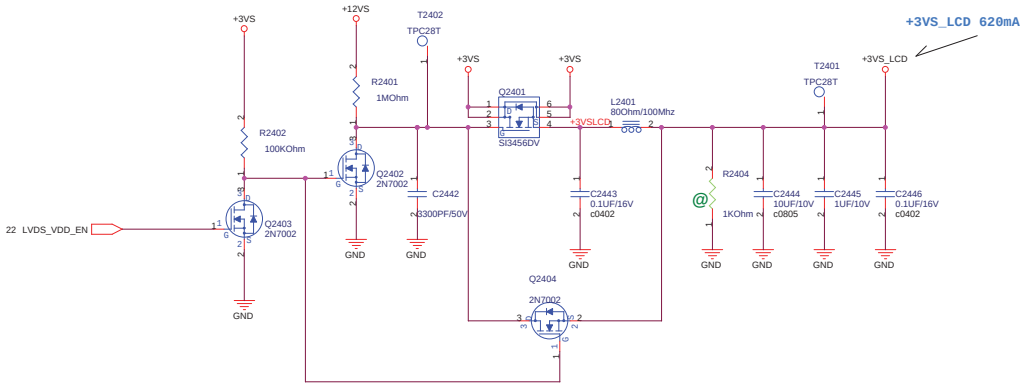


Partition A High 32 bits

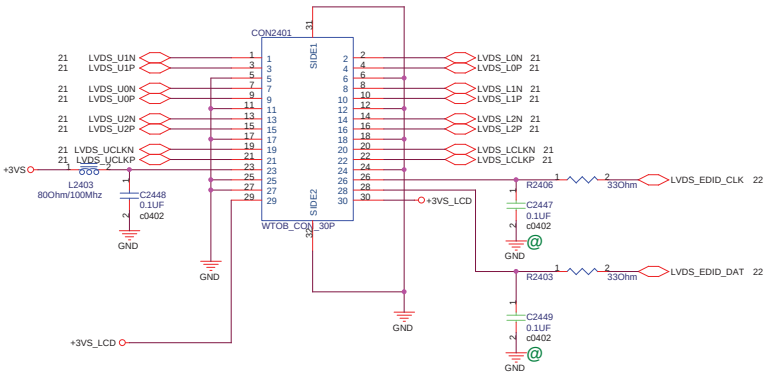
VRAM 64MB delete U2303,U2304



ASUSTek COMPUTER INC NPI	Title : G72M_MEM A		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 0.1
Date: Monday, May 29, 2006	Sheet 23 of 65		

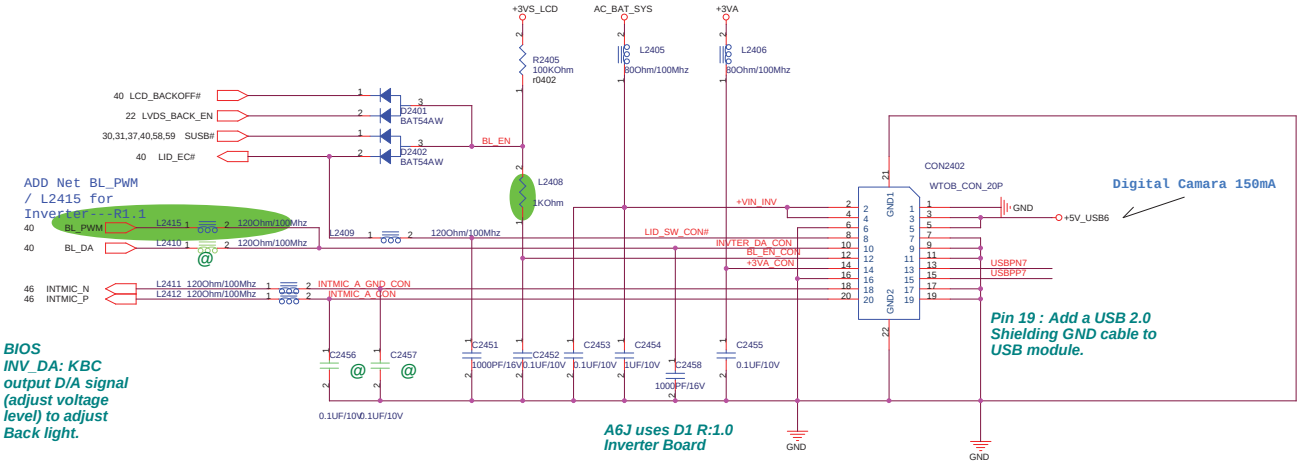


Pin define is the same as A7



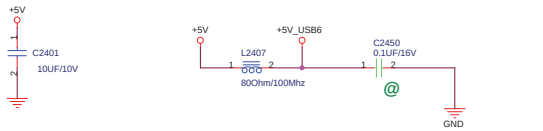
LCD LVDS Interface

BIOS
BACK_OFF#: When user pushs "Fn+F7" button, BIOS activate this pin to turn off back light.

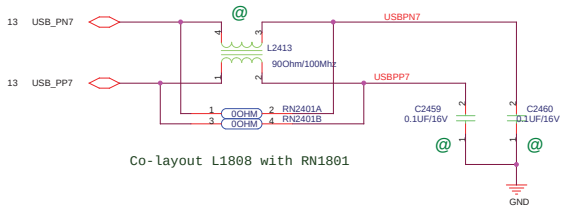


BIOS
INV_DA: KBC output D/A signal (adjust voltage level) to adjust Back light.

A6J uses D1 R:1.0 Inverter Board

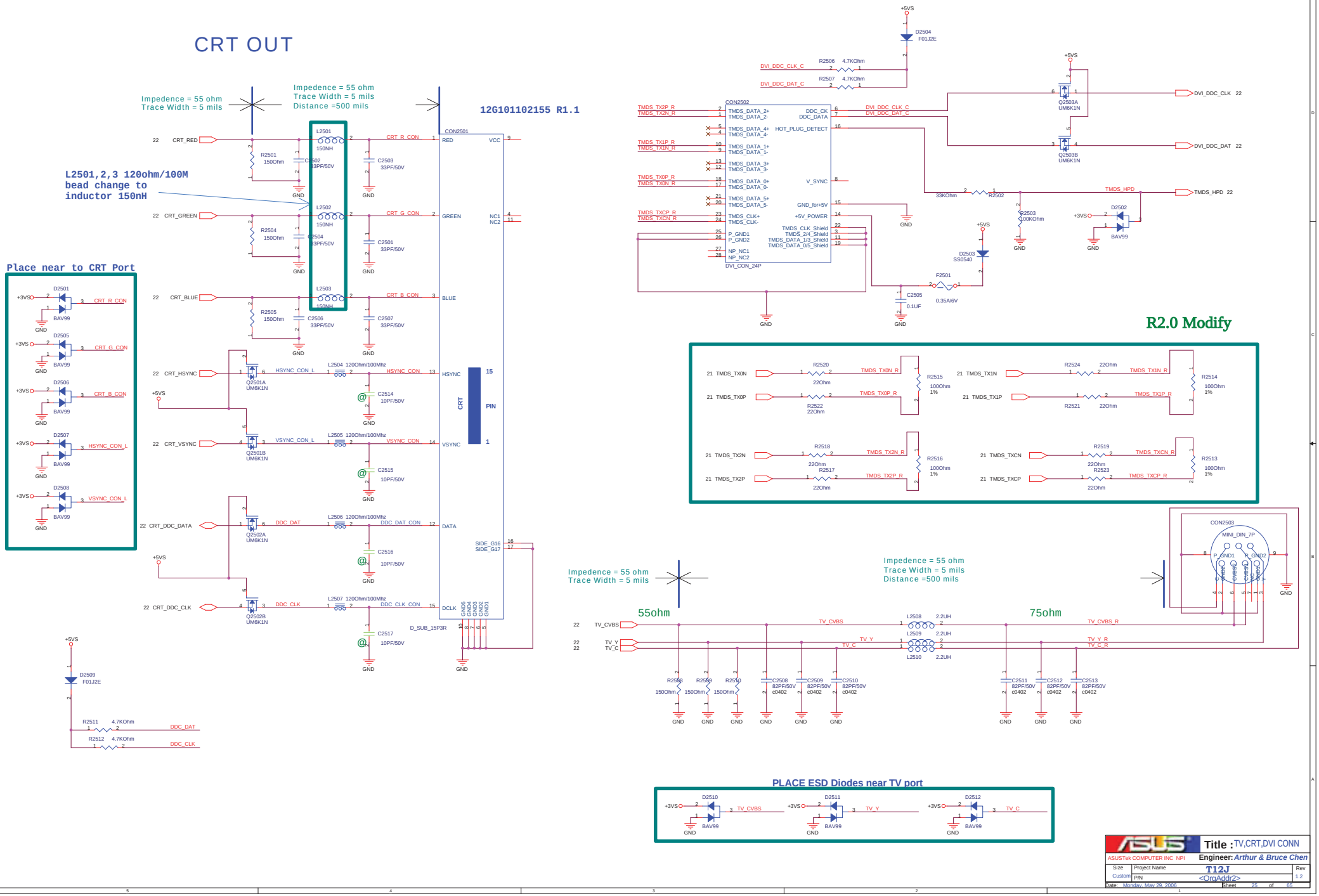


USB PORT 6 for USB CAMERA



ASUSTeK COMPUTER INC NPI	Title : LVDS & INVERTER CONN	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 24 of 65	

CRT OUT



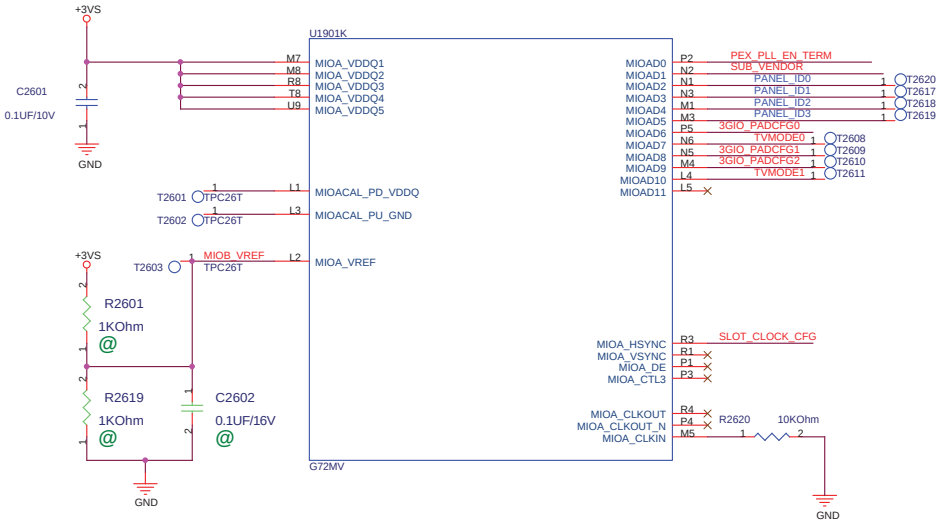
Title : TV,CRT,DVI CONN

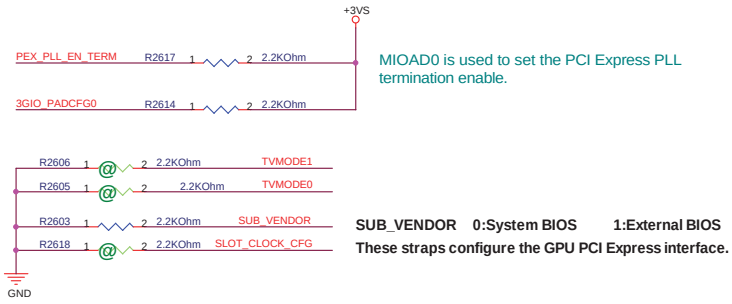
ASUSTek COMPUTER INC NPI

Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	1.2
	P/N: <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 25 of 65

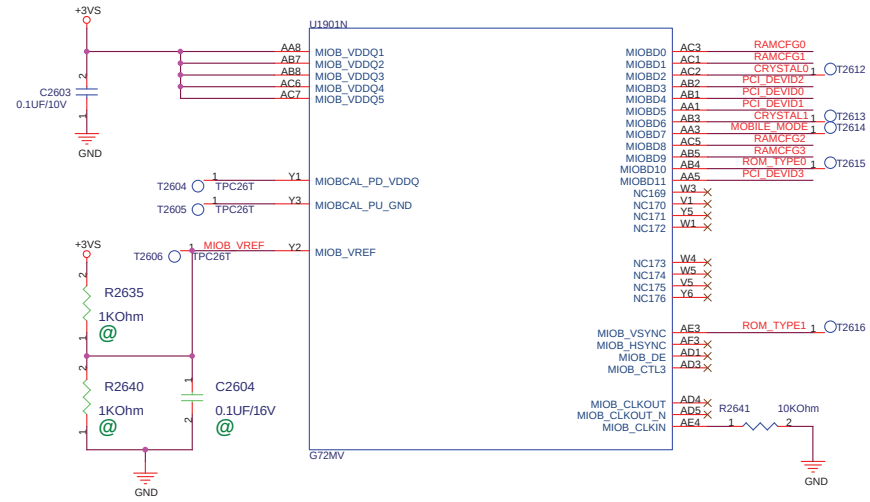


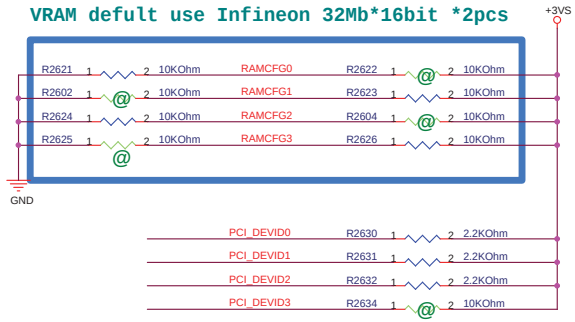


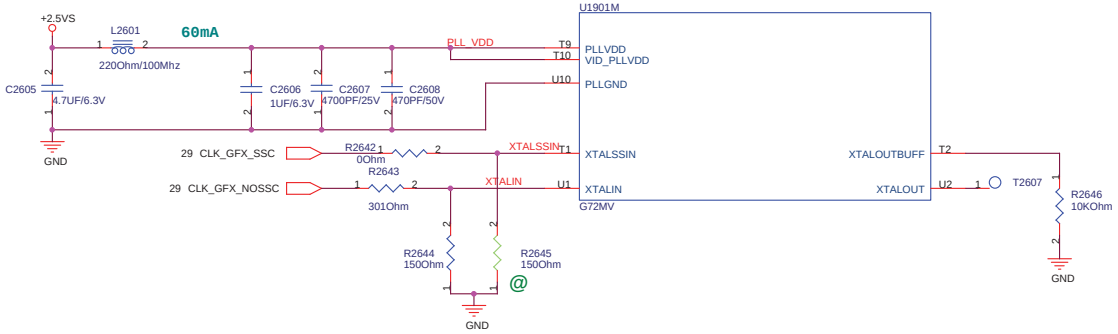
MIOAD0 is used to set the PCI Express PLL termination enable.

SUB_VENDOR 0:System BIOS 1:External BIOS

These straps configure the GPU PCI Express interface.







PANEL_ID[3:0] 1XXX:Customer Defined

TVMODE[1:0]
- 00:SECAM
- 01:NTSC
- 10:PAL
- 11:VGA

3GIO_PADCFG[2:0] 001:For G7x

RAMCFG[2:0]
- 0001:16M x 16 DDR2 64-bit Samsung
- 0010:16M x 16 DDR2 64-bit Infineon
- 0011:16M x 16 DDR2 64-bit Hynix
- 0101:32M x 16 DDR2 64-bit Samsung
- 0110:32M x 16 DDR2 64-bit Infineon
- 0111:32M x 16 DDR2 64-bit Hynix

RAMCFG3
- 0:Full width of the frame buffer
- 1:Half width of the frame buffer

CRYSTAL[1:0] 10:27.0MHz

PCI_DEVID[3:0]
- 0111:G72M-V
- 1000:G72M

ROM_TYPE[1:0]
- 00:Parallel
- 01:Serial
- 10:Reserved
- 11:LPC

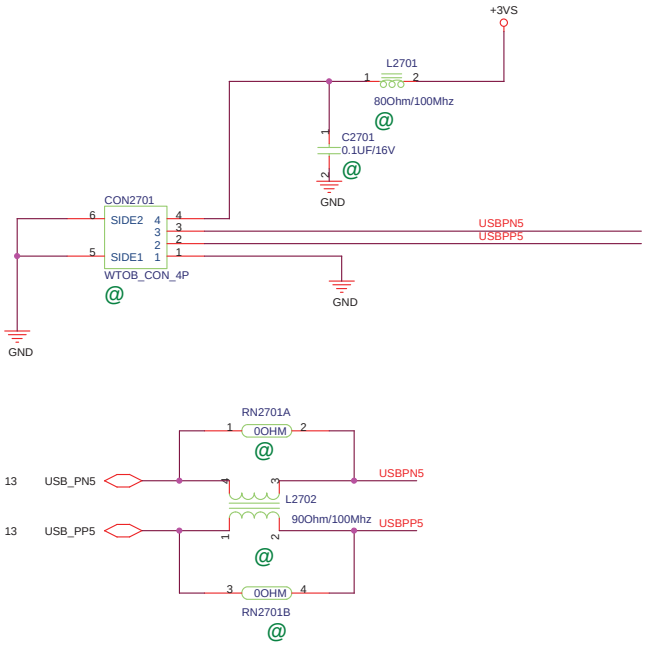
ASUSTek COMPUTER INC NPI

Title : G72M_STRAP/XTAL

Engineer: *Arthur & Bruce Chen*

Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 26 of 65



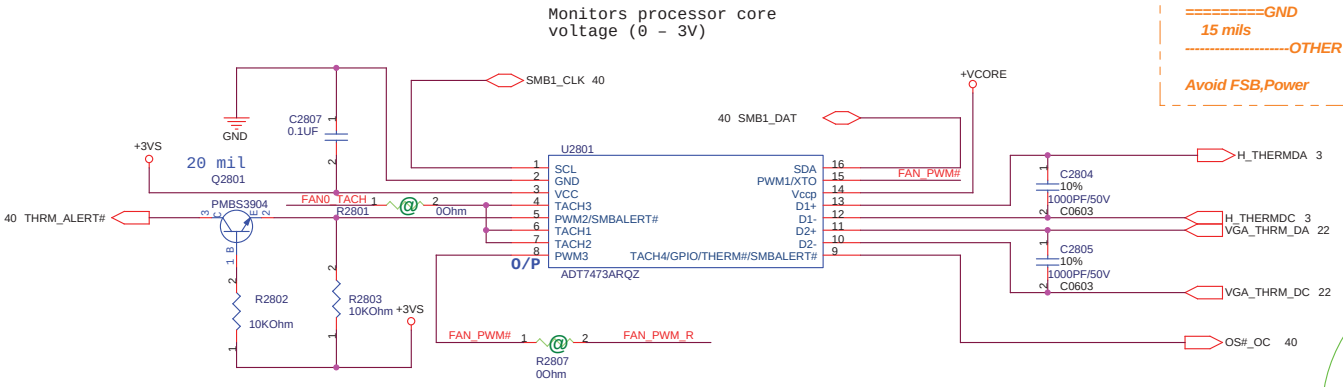
ASUSTek COMPUTER INC NPI	Title : FINGER PRINT		
	Engineer: *Arthur & Bruce Chen*		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 27 of 65		

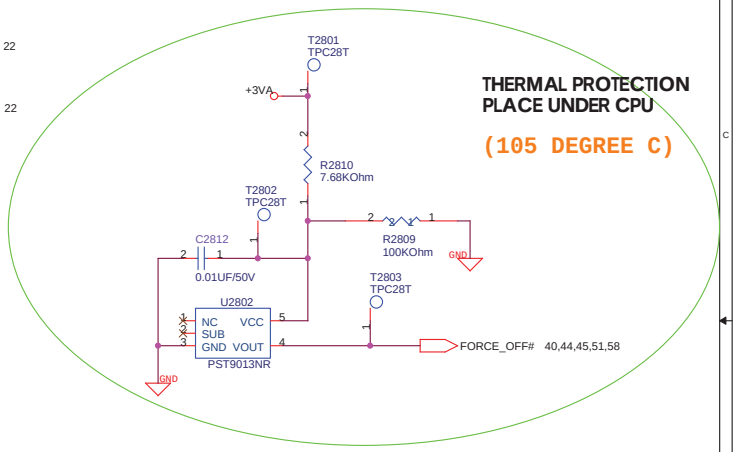
Thermal Sensor

Route H_THERMDA and H_THERMDC on the same layer

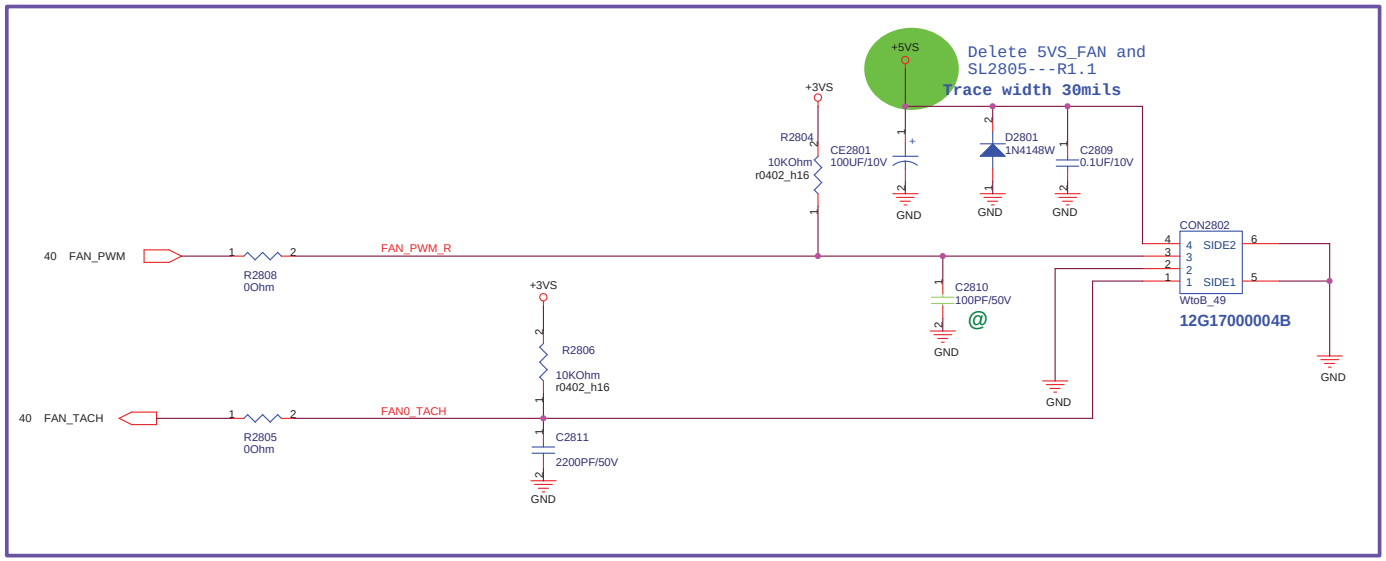
----------OTHER SIGNALS
15 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
15 mils
----------OTHER SIGNALS

Avoid FSB,Power





DC FAN Control



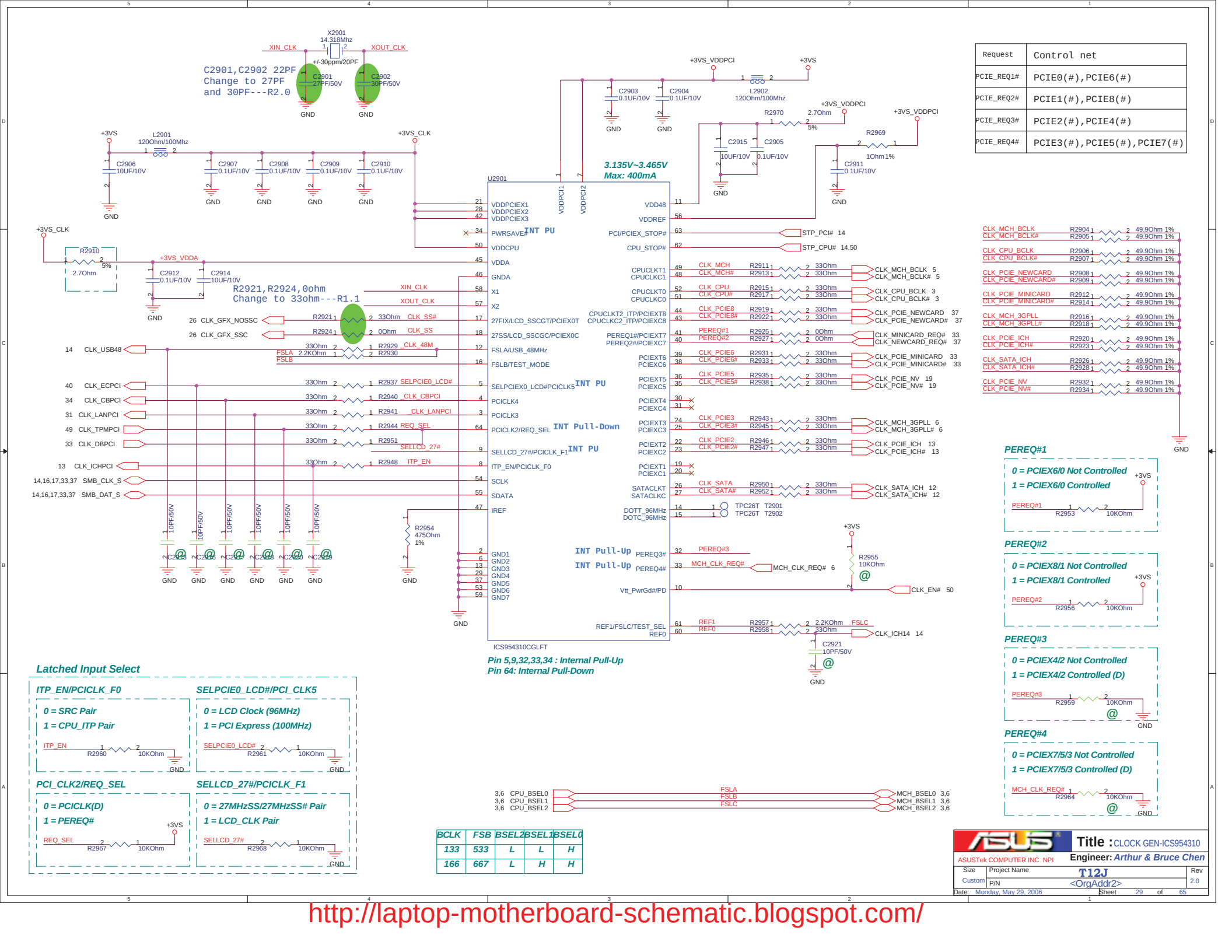
ASUSTek COMPUTER INC NPI

Title : THER SENSOR & FAN

Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	2.0
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 28 of 65



Request	Control net
PCIE_REQ1#	PCIE0(#),PCIE6(#)
PCIE_REQ2#	PCIE1(#),PCIE8(#)
PCIE_REQ3#	PCIE2(#),PCIE4(#)
PCIE_REQ4#	PCIE3(#),PCIE5(#),PCIE7(#)

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

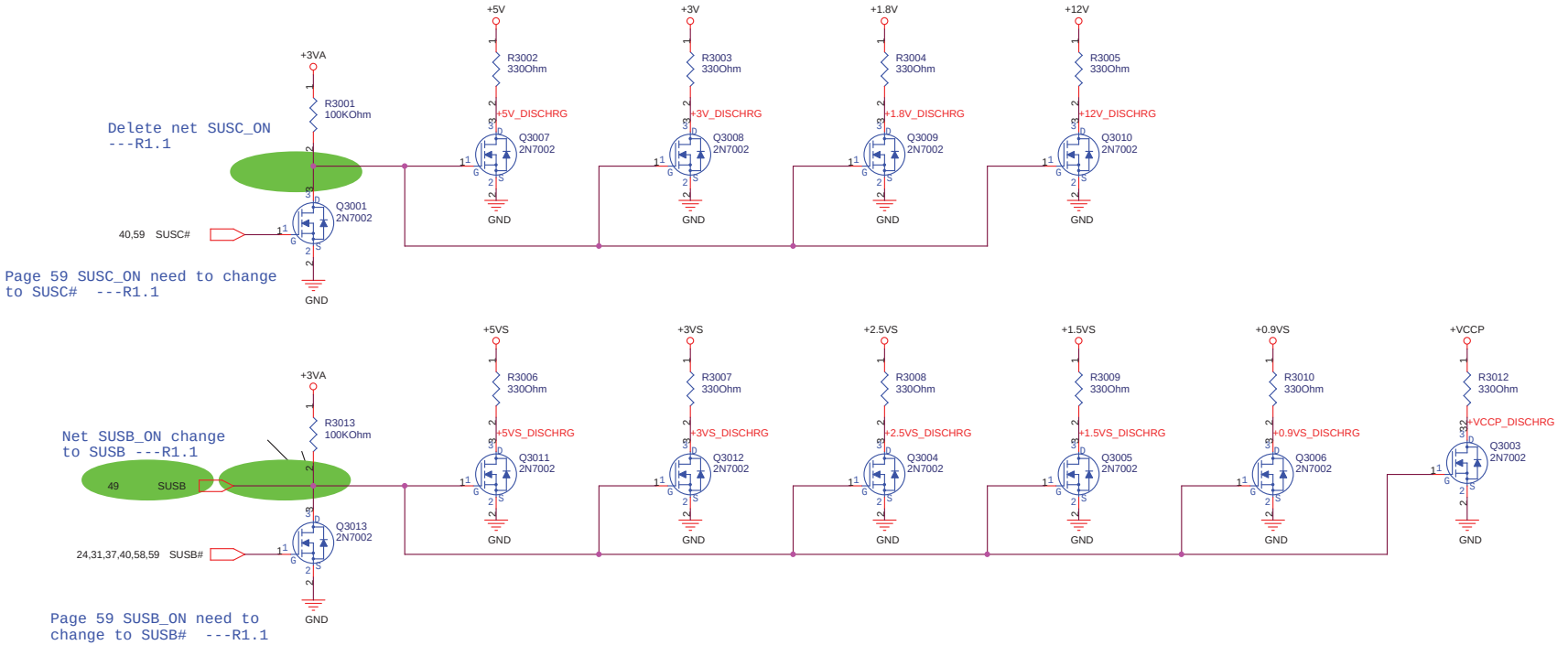
ASUSTek COMPUTER INC NPI

Title : CLOCK GEN-ICS954310

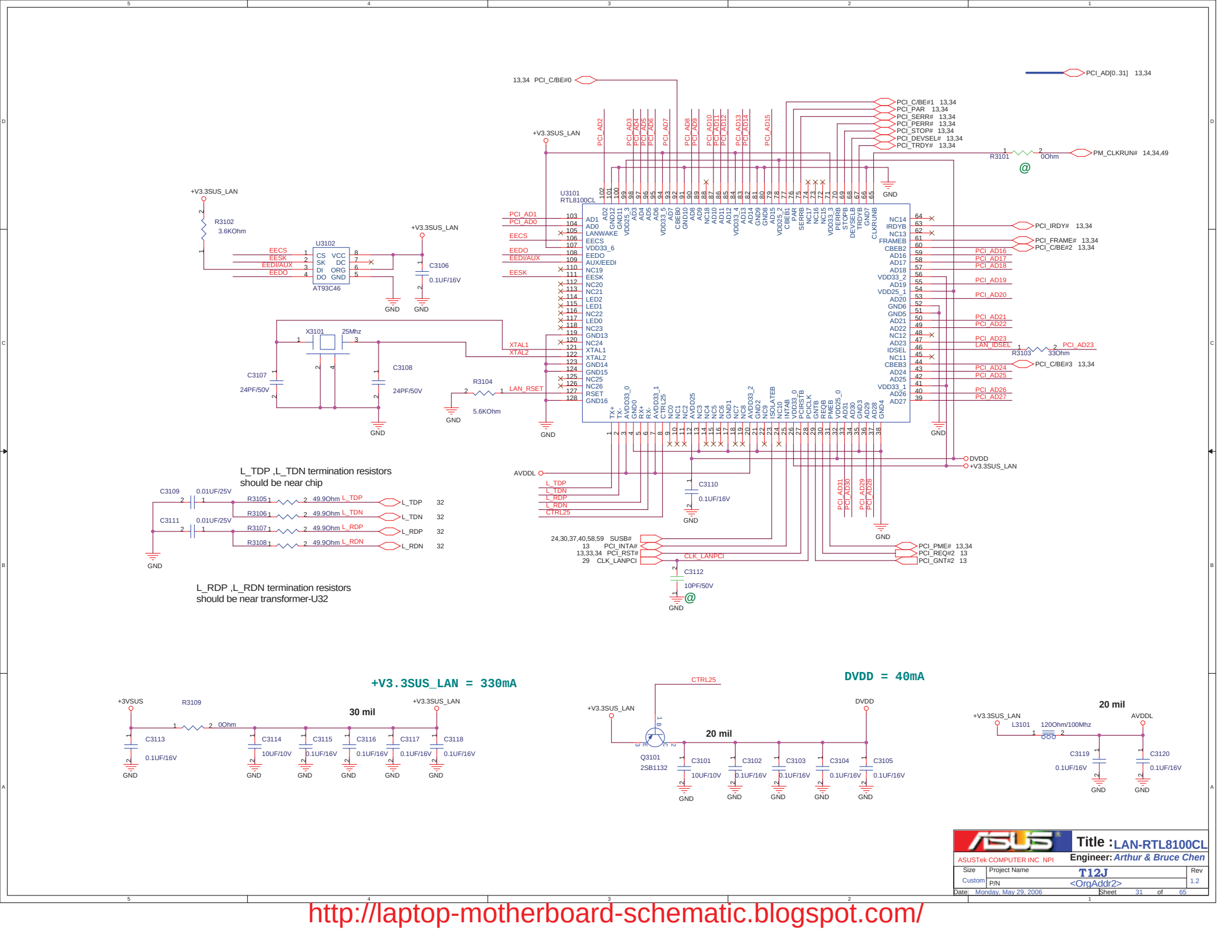
Engineer: Arthur & Bruce Chen

Size	Project Name	Rev
Custom	T12J	2.0
	P/N <OrgAddr2>	

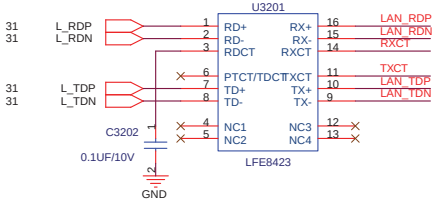
Date: Monday, May 29, 2006 Sheet 29 of 65



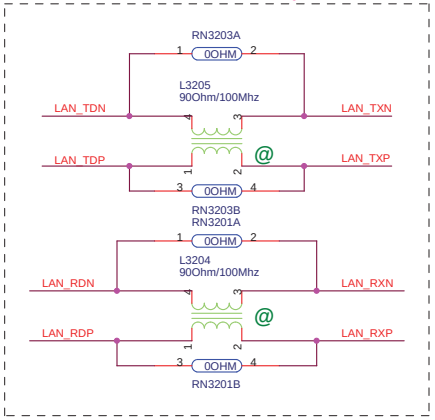
Title : DISCHARGE & EMI CAP		
ASUSTek COMPUTER INC NPI	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 30 of 65	

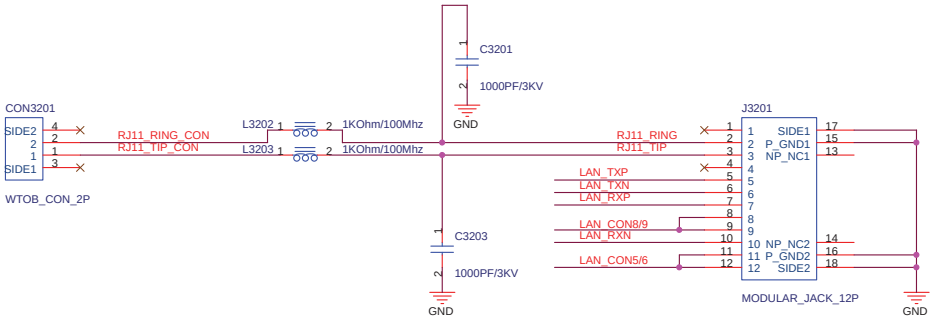


RJ11&RJ45 Port

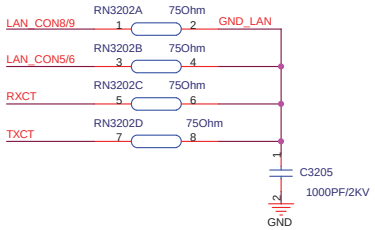


FOR EMI Co-Lay

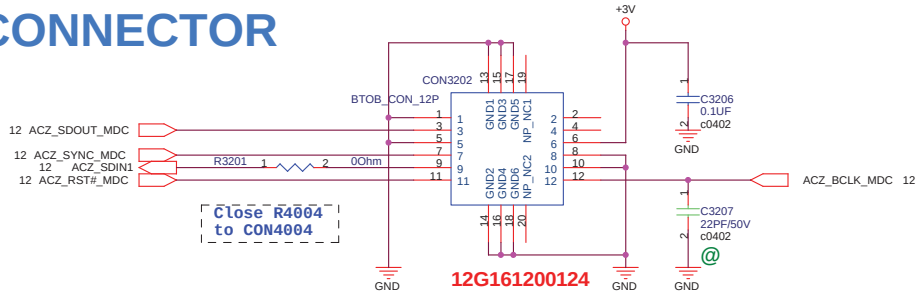




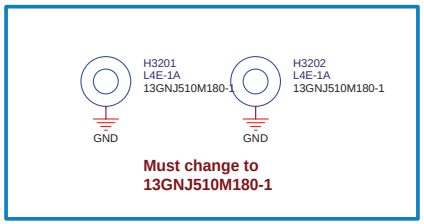
Change
12G142111120 R1.1



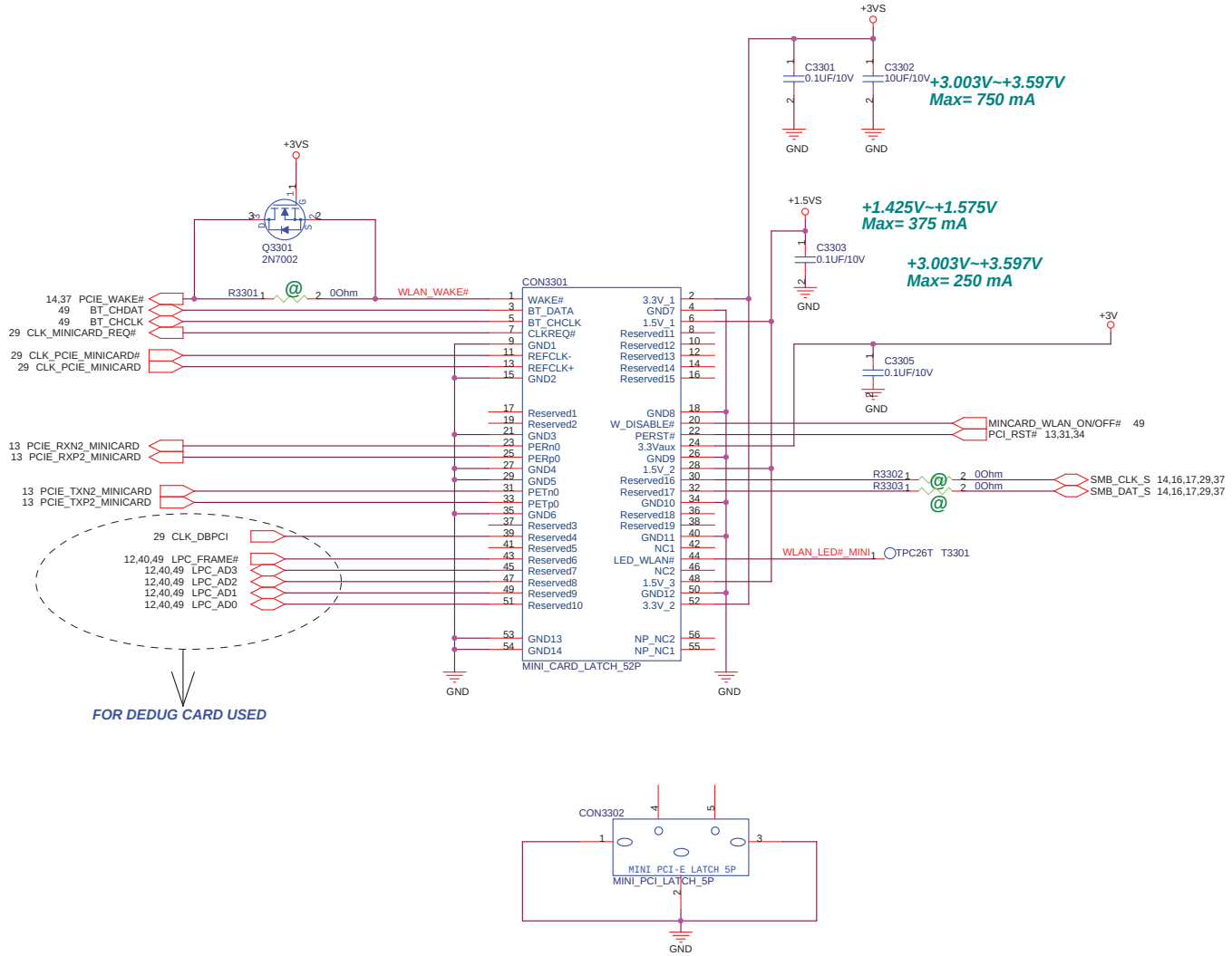
MDC CONNECTOR



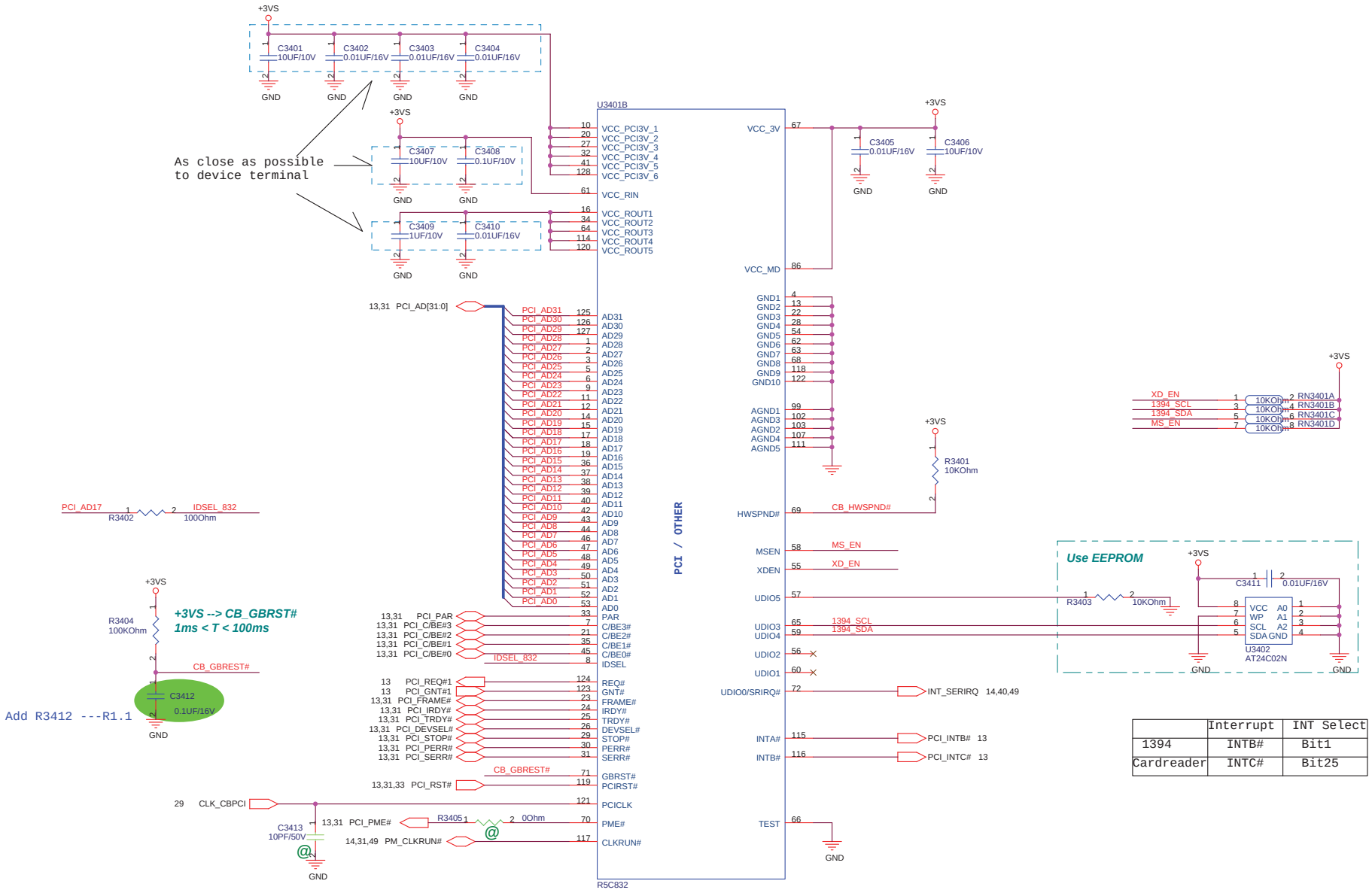
Close R4004
to CON4004

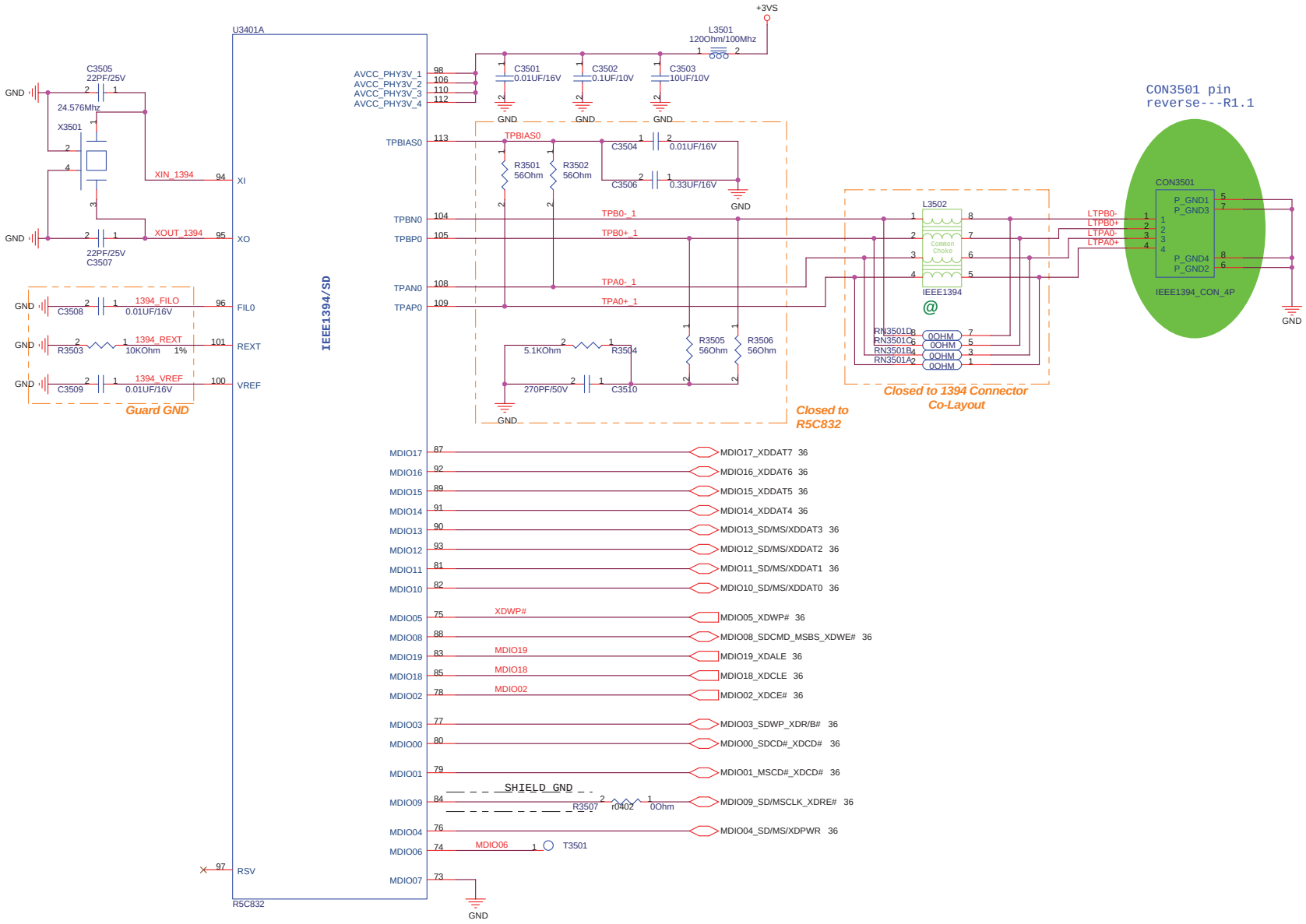


ASUSTek COMPUTER INC NPI	Title : MDC & RJ45+11	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 32 of 65	

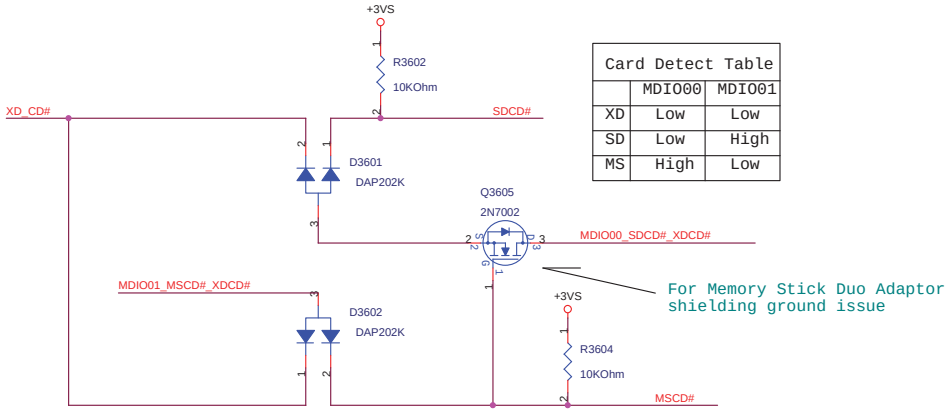


ASUSTek COMPUTER INC NPI	Title : MINICARD	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 2.0
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 33 of 65	



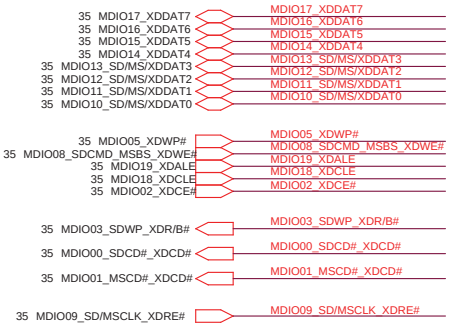


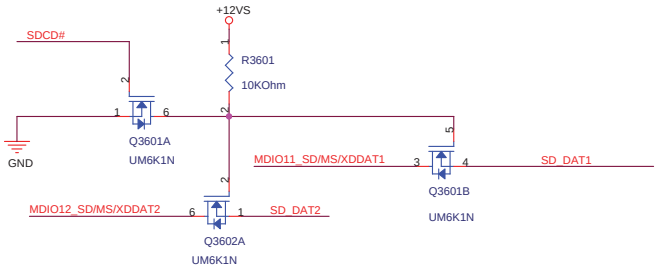
ASUSTek COMPUTER INC NPI	Title : R5C832-1394(2)	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 35 of 65	

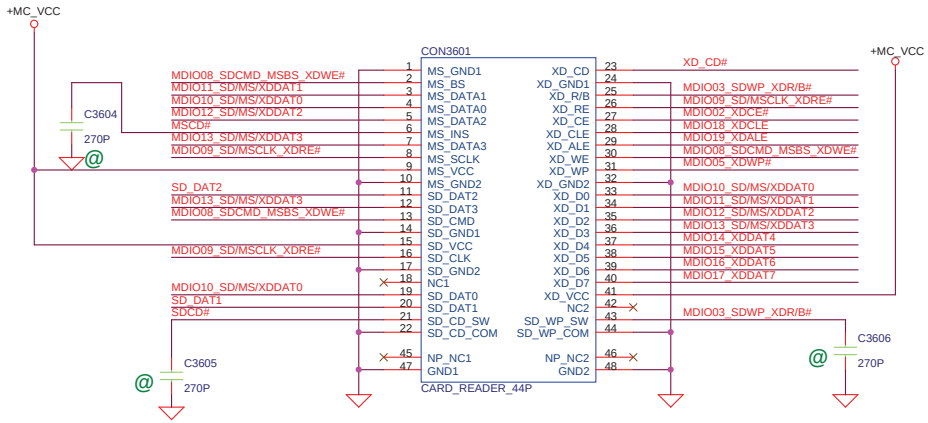


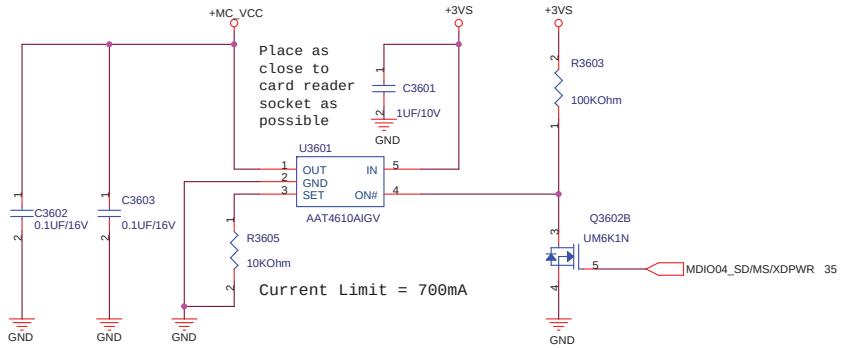
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU









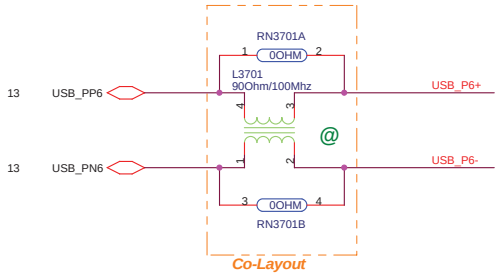
ASUSTek COMPUTER INC NPI

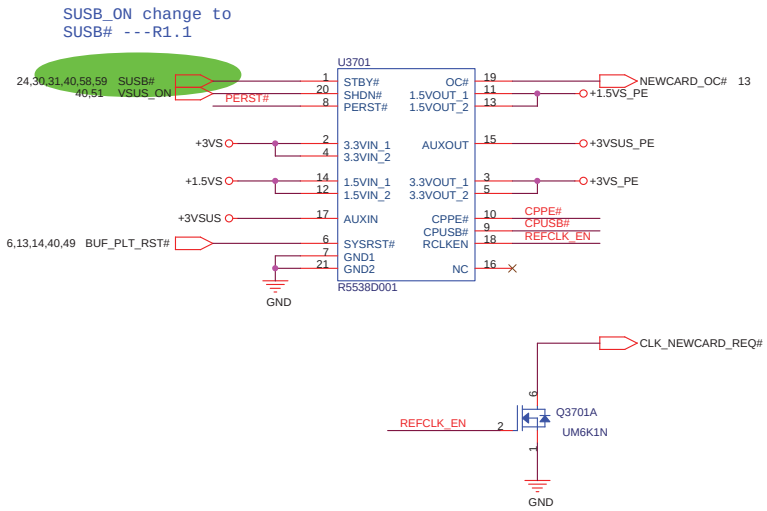
Title : 4 in 1 CARD READER

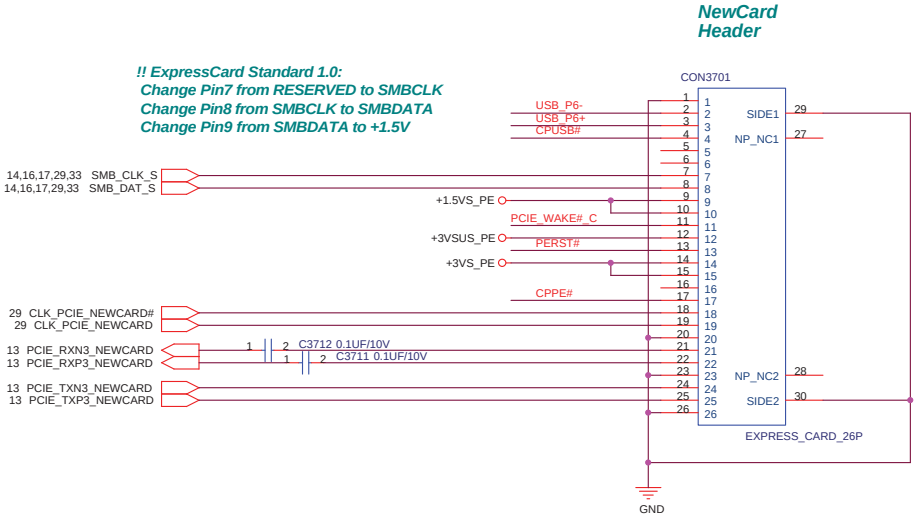
Engineer: Arthur & Bruce Chen

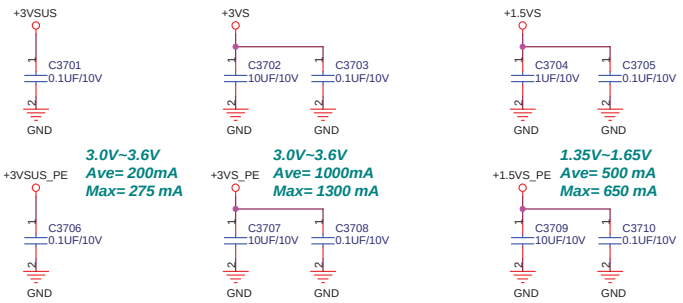
Size	Project Name	Rev
Custom	T12J	1.2
	P/N <OrgAddr2>	

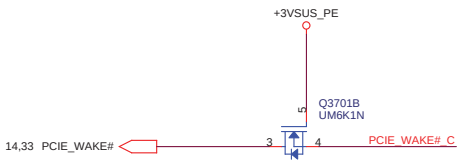
Date: Monday, May 29, 2006 Sheet 36 of 65

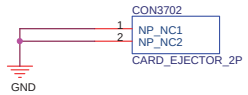




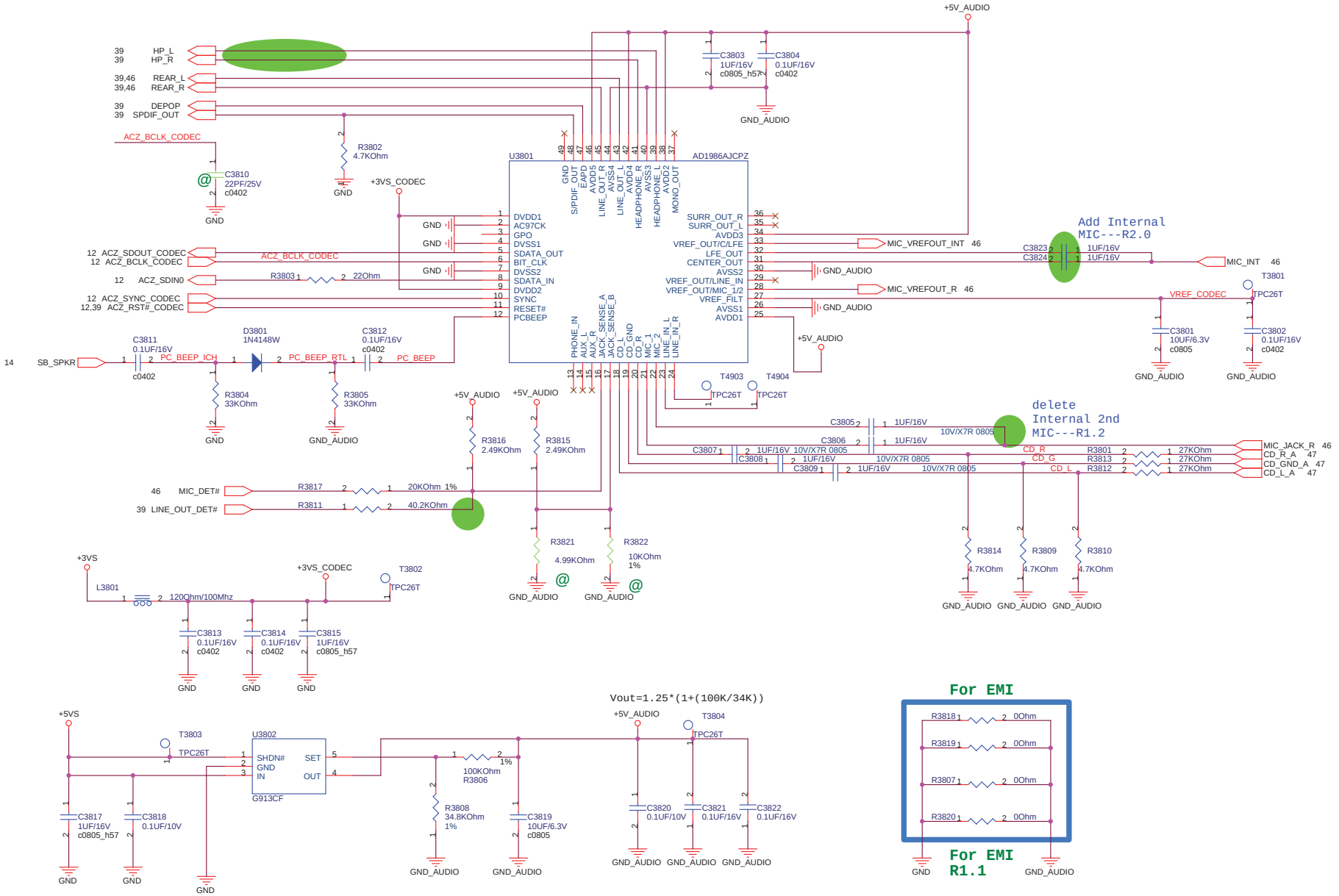




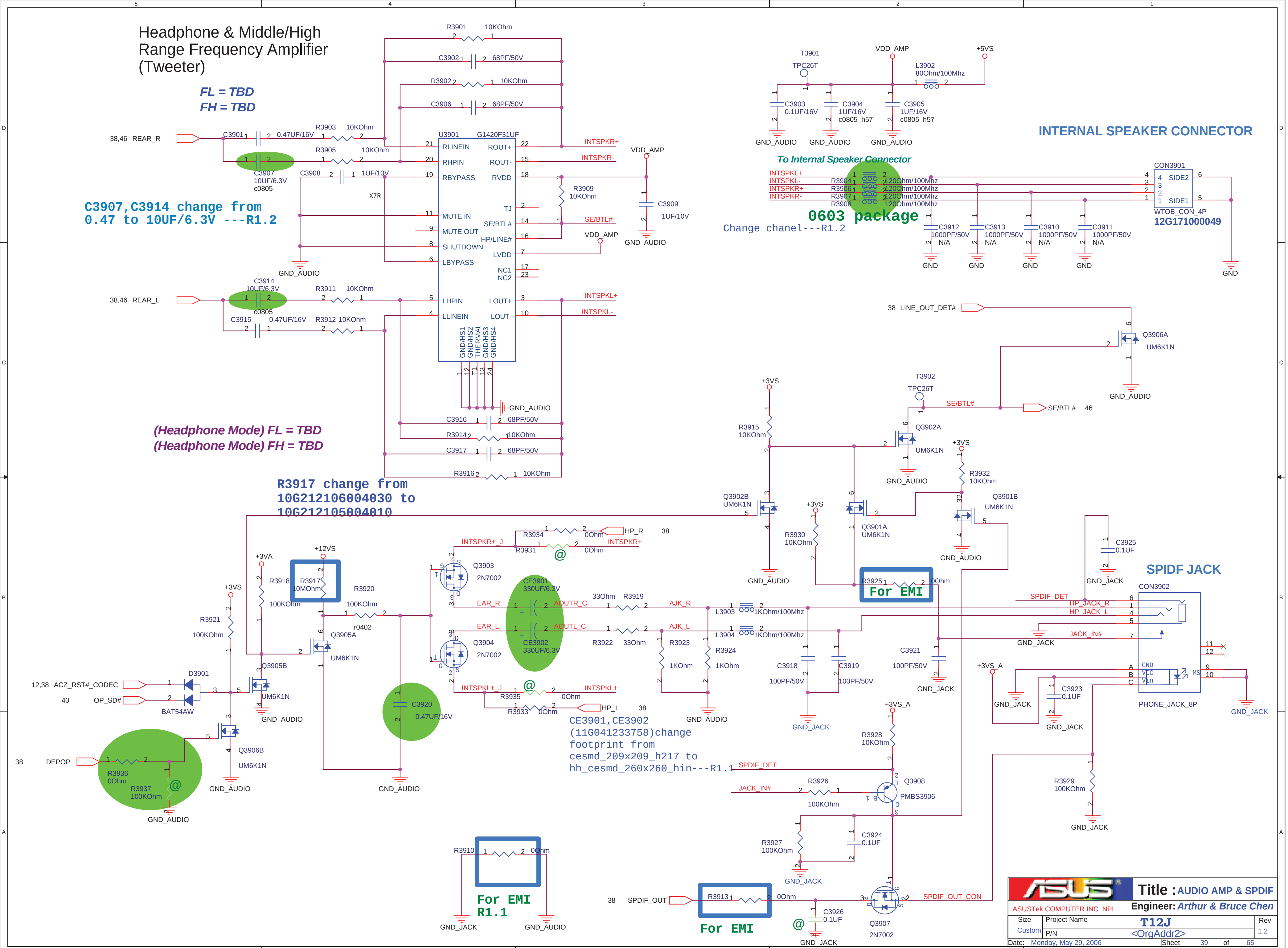




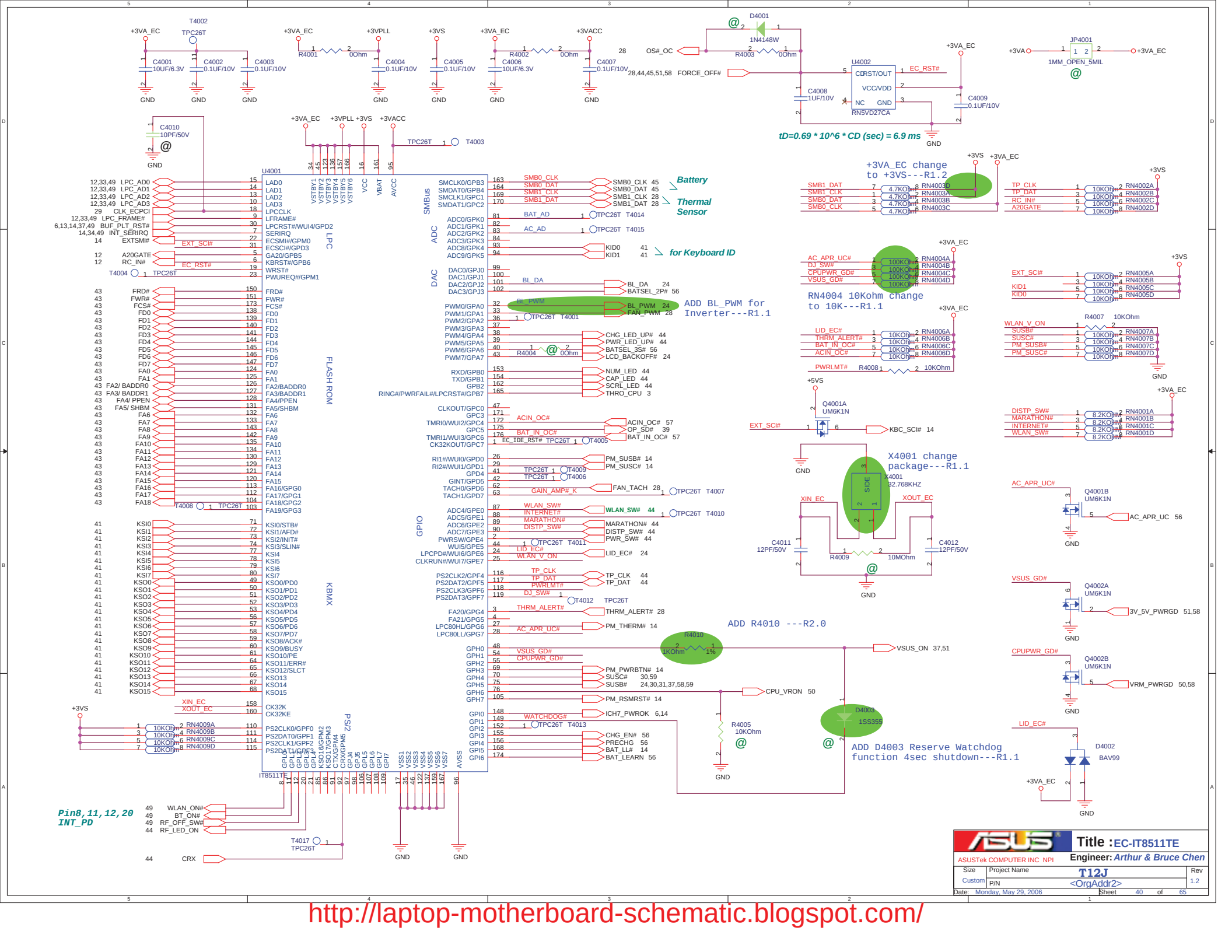
ASUSTek COMPUTER INC NPI	Title : NEWCARD	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 37 of 65	



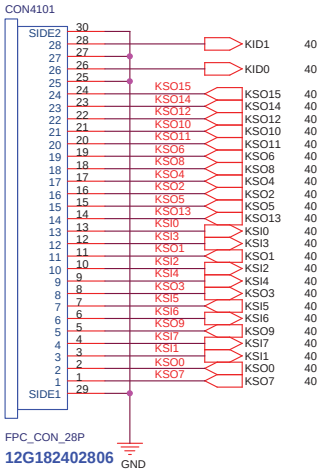
ASUSTek COMPUTER INC NPI	Title : AUDIO-AD1986A		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 38 of 65		



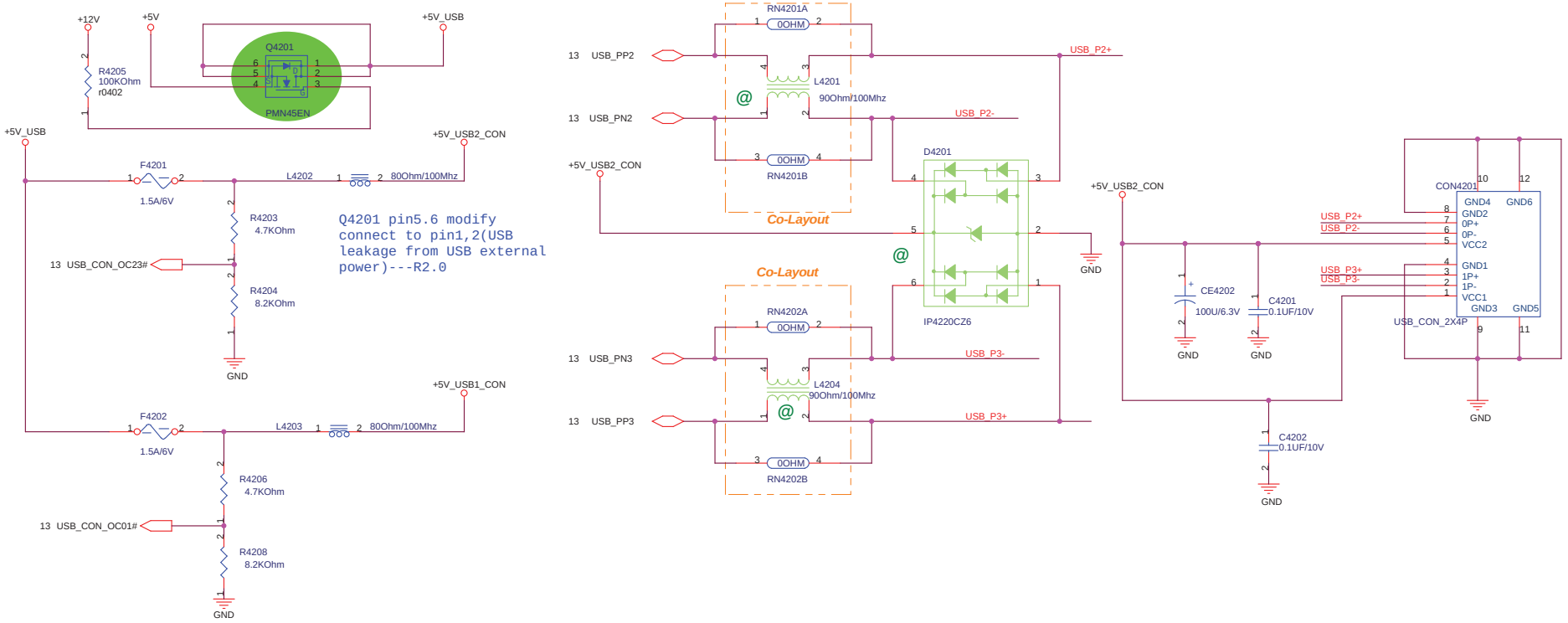
http://laptop-motherboard-schematic.blogspot.com/

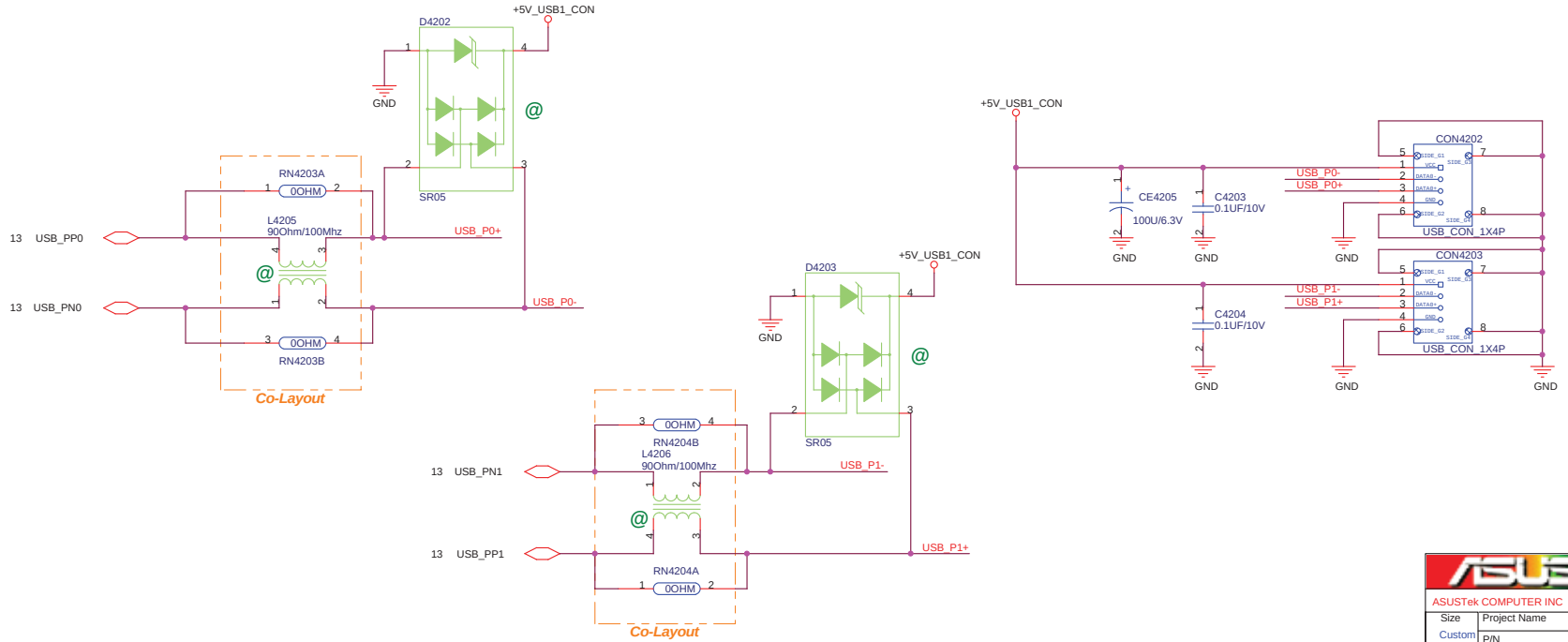

U4001
IT8511TE
LPC
FLASH ROM
KBMX
PS/2
GPIO
ADC
DAC
SMBus
Battery
Thermal Sensor
for Keyboard ID
ADD BL_PWM for Inverter---R1.1
+3VA_EC change to +3VS---R1.2
RN4004 10Kohm change to 10K---R1.1
X4001 change package---R1.1
ADD R4010 ---R2.0
ADD D4003 Reserve Watchdog function 4sec shutdown---R1.1
tD=0.69 * 10^6 * CD (sec) = 6.9 ms
Pin8,11,12,20 INT_PD
Title : EC-IT8511TE
ASUSTek COMPUTER INC NPI
Engineer: Arthur & Bruce Chen
T12J
Monday, May 29, 2006
http://laptop-motherboard-schematic.blogspot.com/

For Keyboard
Metrix Define same Z94



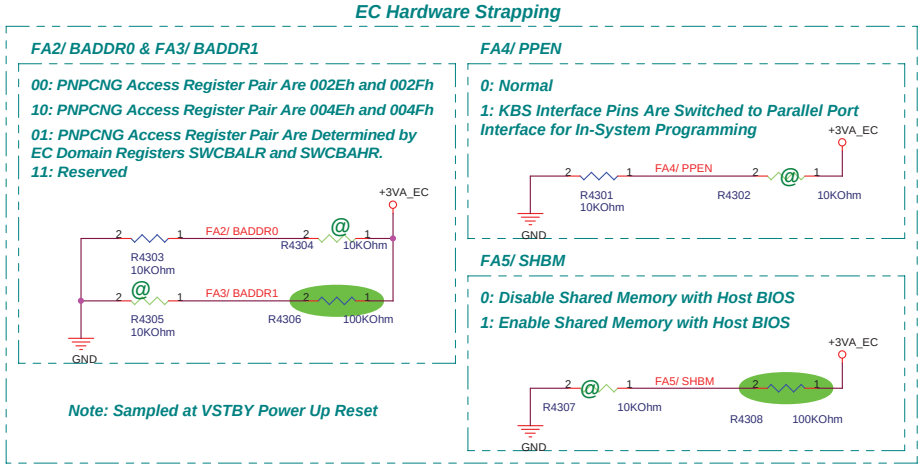
Title : Keyboard CONN		
ASUSTek COMPUTER INC NPI	Engineer: *Arthur & Bruce Chen*	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 41 of 65	



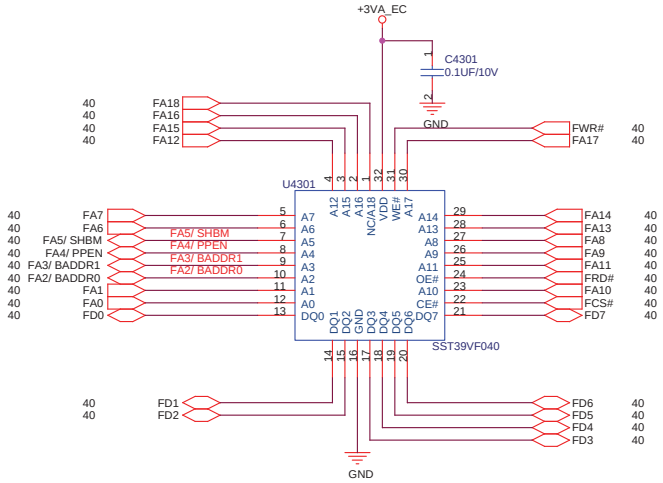


ASUSTek COMPUTER INC NPI	Title : USB CONN	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 42 of 65	

ISA ROM

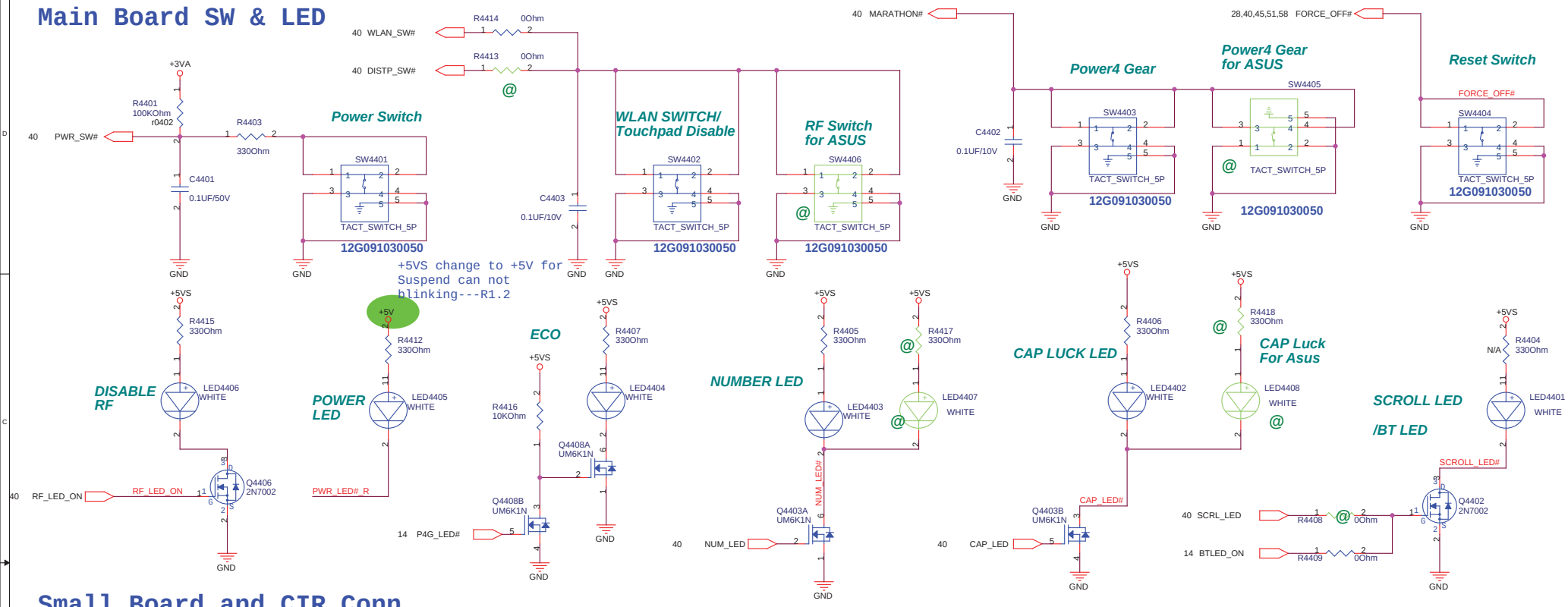


R4306,R4308 10Kohm change to 100Kohm---R1.2



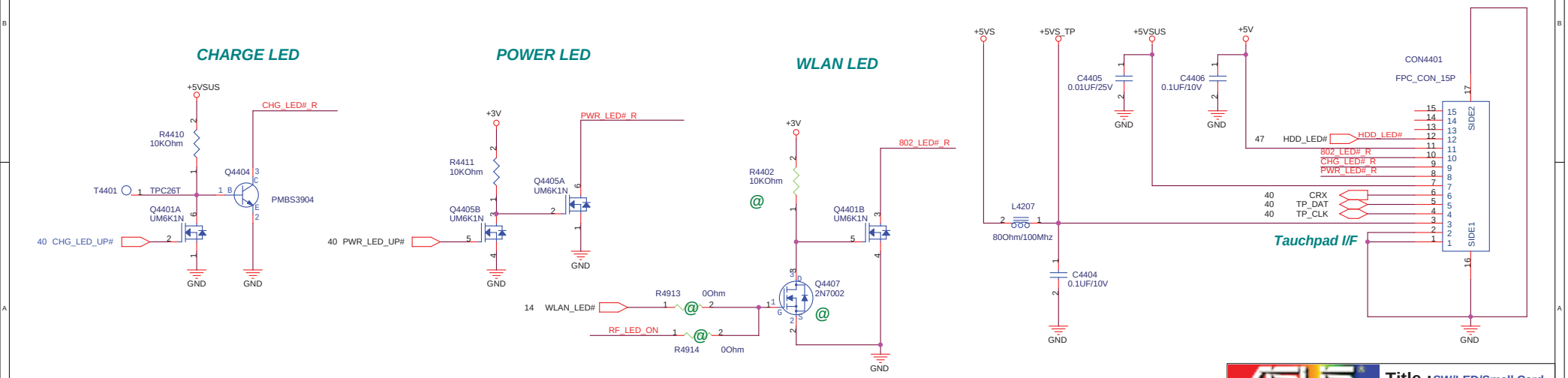
ASUSTek COMPUTER INC NPI	Title : ISA ROM		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J	P/N: <OrgAddr2>	Rev: 1.2
Date: Monday, May 29, 2006	Sheet 43 of 65		

Main Board SW & LED



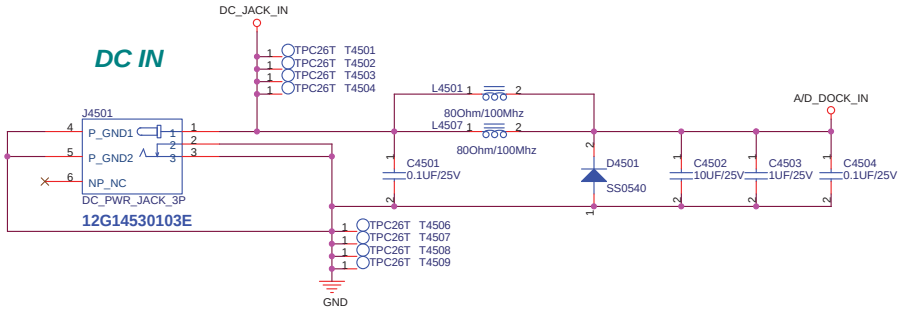
Small Board and CIR Conn.

LED Board Connector



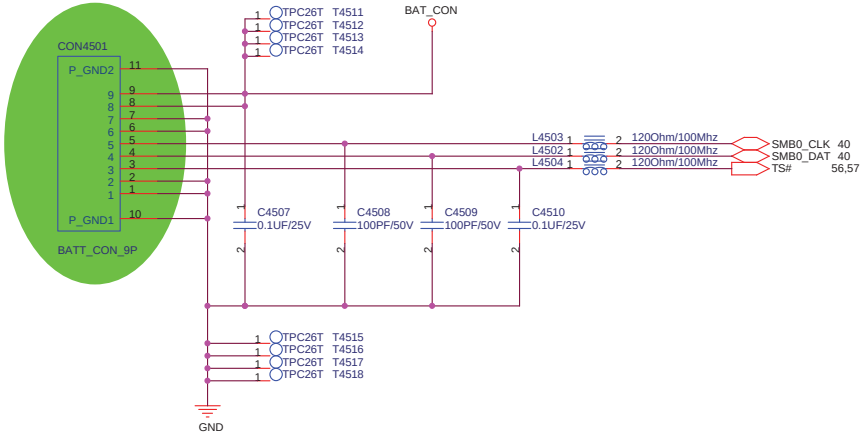
ASUSTek COMPUTER INC NPI	Title : SW/LED/Small Card	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 44 of 65	

DC IN



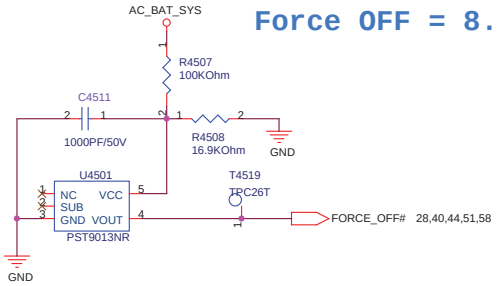
BAT IN

CON4501 change package---R1.1

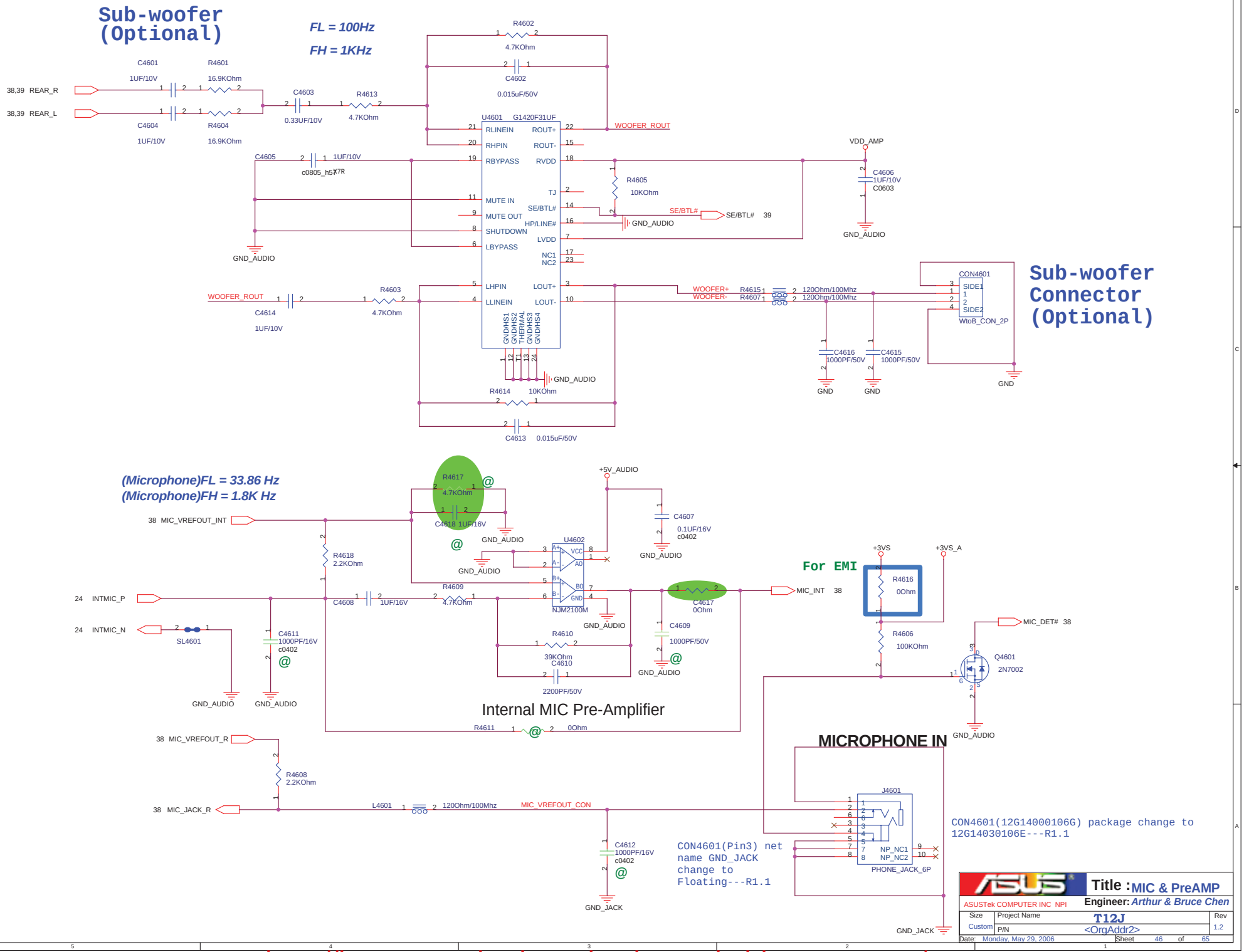


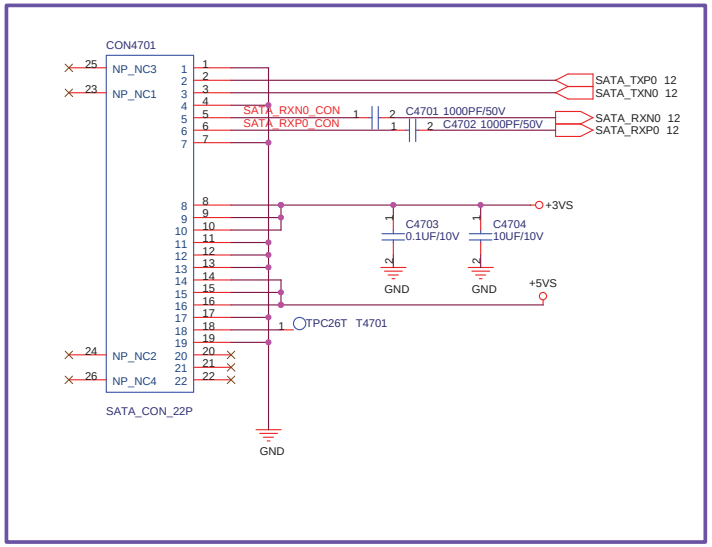
Without Battery & Pull out Adapter

Force OFF = 8.99V



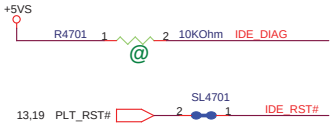
ASUSTek COMPUTER INC NPI	Title : DC & BAT IN	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 0.1
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 45 of 65	



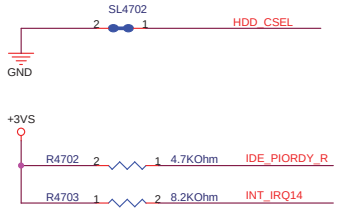


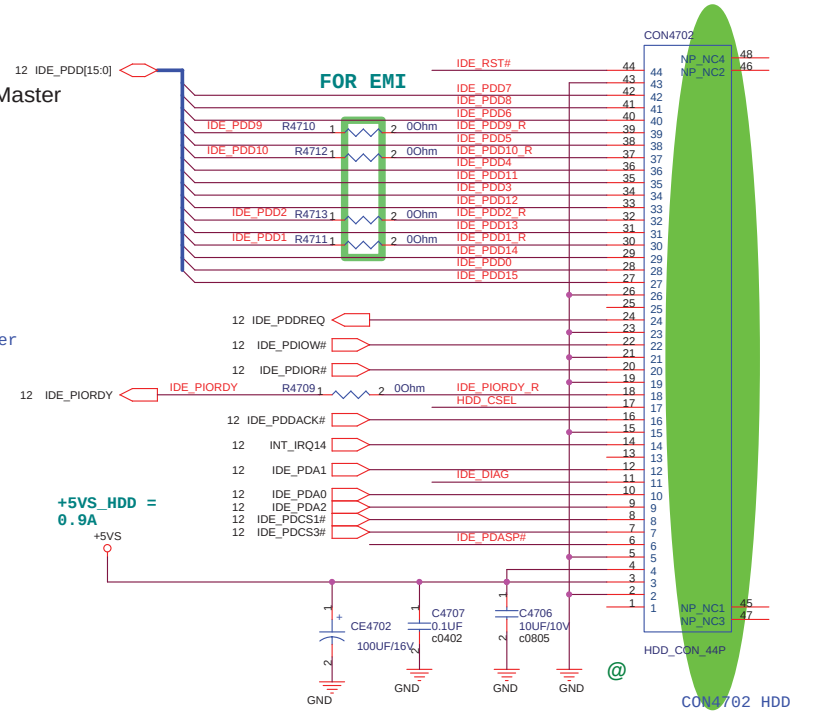
SATA HDD

HD_CSEL : Pull-Down, HDD as Master



HDD_CSEL : Pull-Down HDD as Master



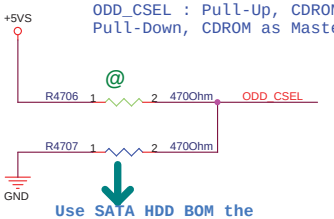


CON4702 HDD connector reverse---R1.1

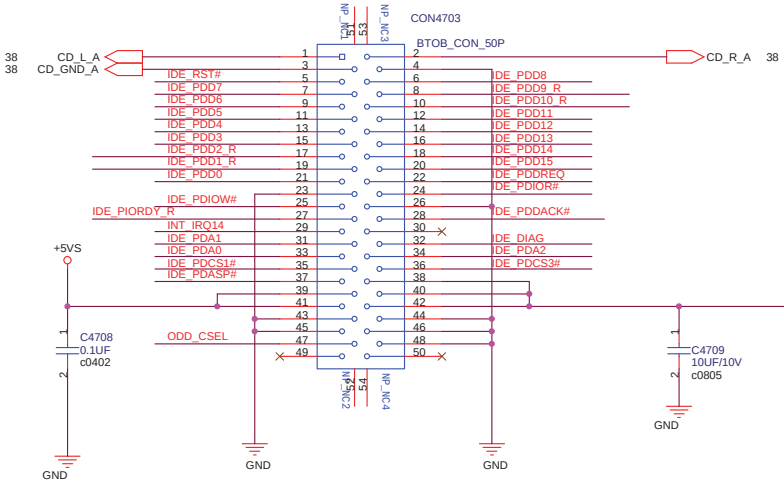
PATA HDD

CD-ROM

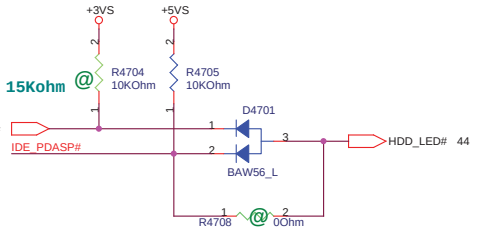
ODD_CSEL : Pull-Up, CDROM as Slave, Pull-Down, CDROM as Master



Use SATA HDD BOM the ODD select R4707(Secondary Master)

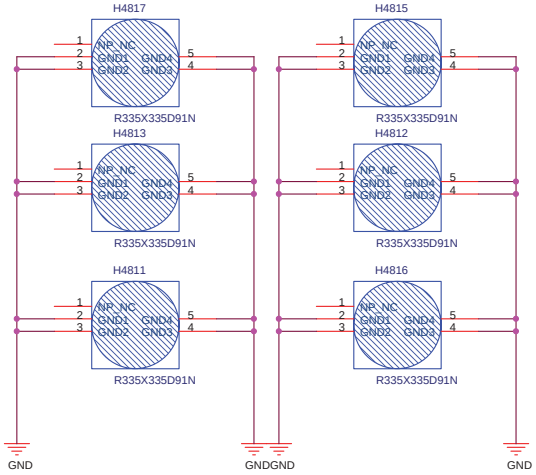


ICH: Int PU 15Kohm

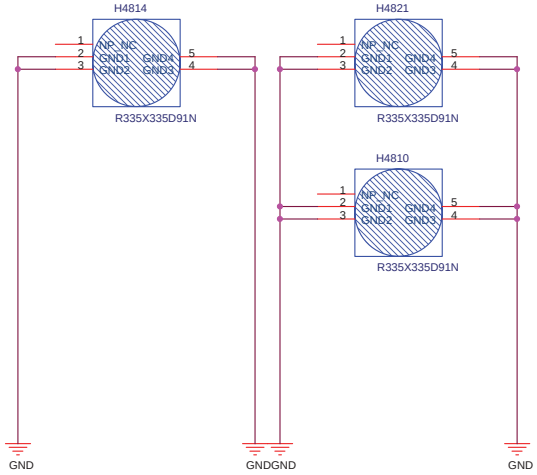


ASUSTek COMPUTER INC NPI	Title : SATA-HDD & ODD	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 1.2
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 47 of 65	

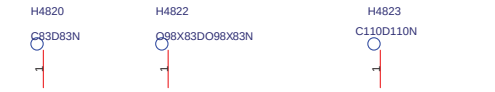
A Hole / TOP Side



A Hole / Bottom Side

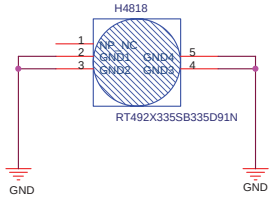


Drill Hole for Fix

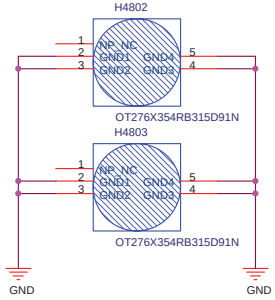


圓孔　　橢圓孔　　圓孔New R1.1

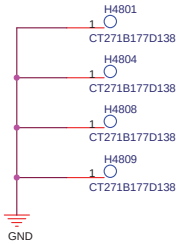
A Hole Special / Bottom Side



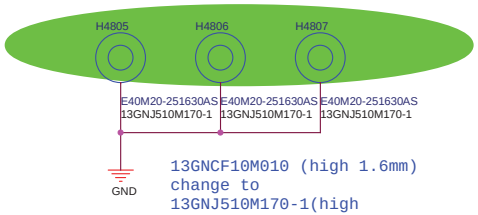
E Hole for Main board fix



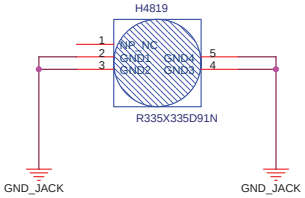
F Hole for CPU



銅柱 Hole for VGA 13GNJ510M170-1

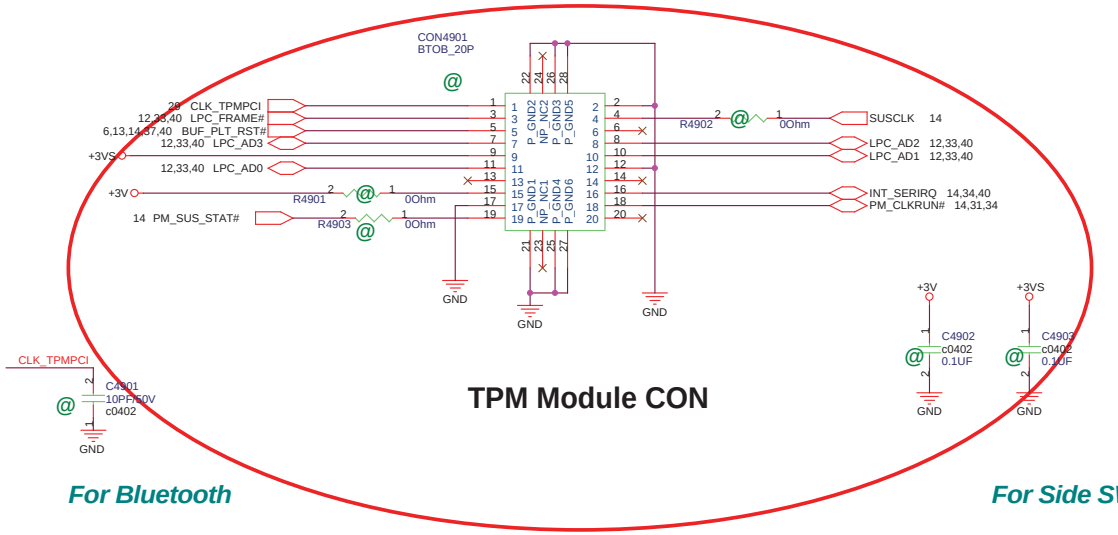


13GNCF10M010 (high 1.6mm) change to 13GNJ510M170-1(high 1.2mm)---R1.1

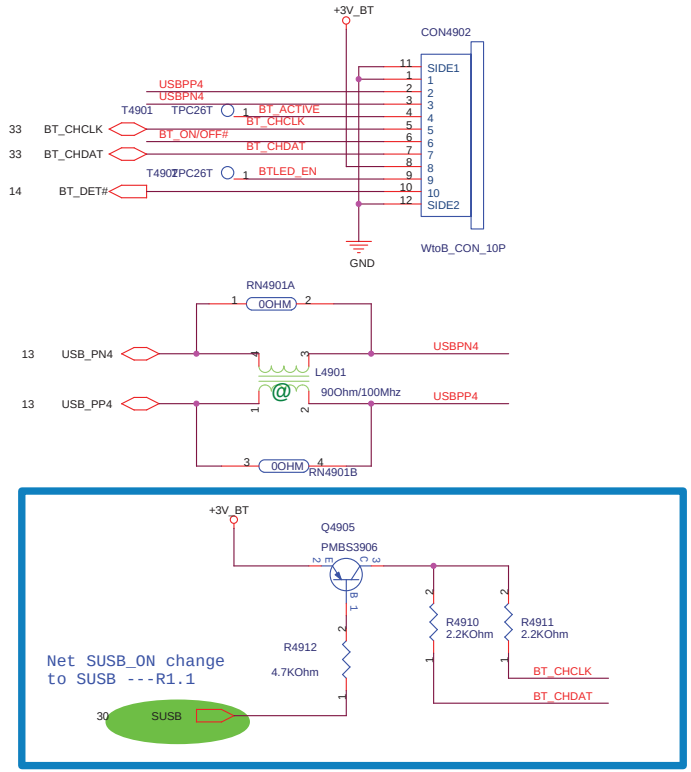


ASUSTek COMPUTER INC NPI	Title : SREW HOLE	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 0.1
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 48 of 65	

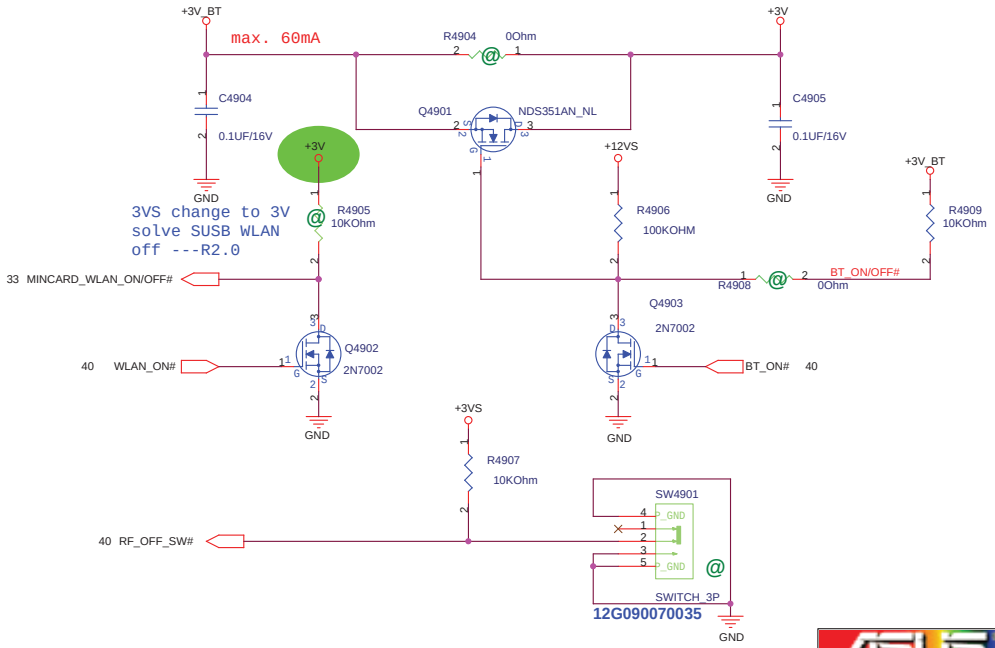
TPM



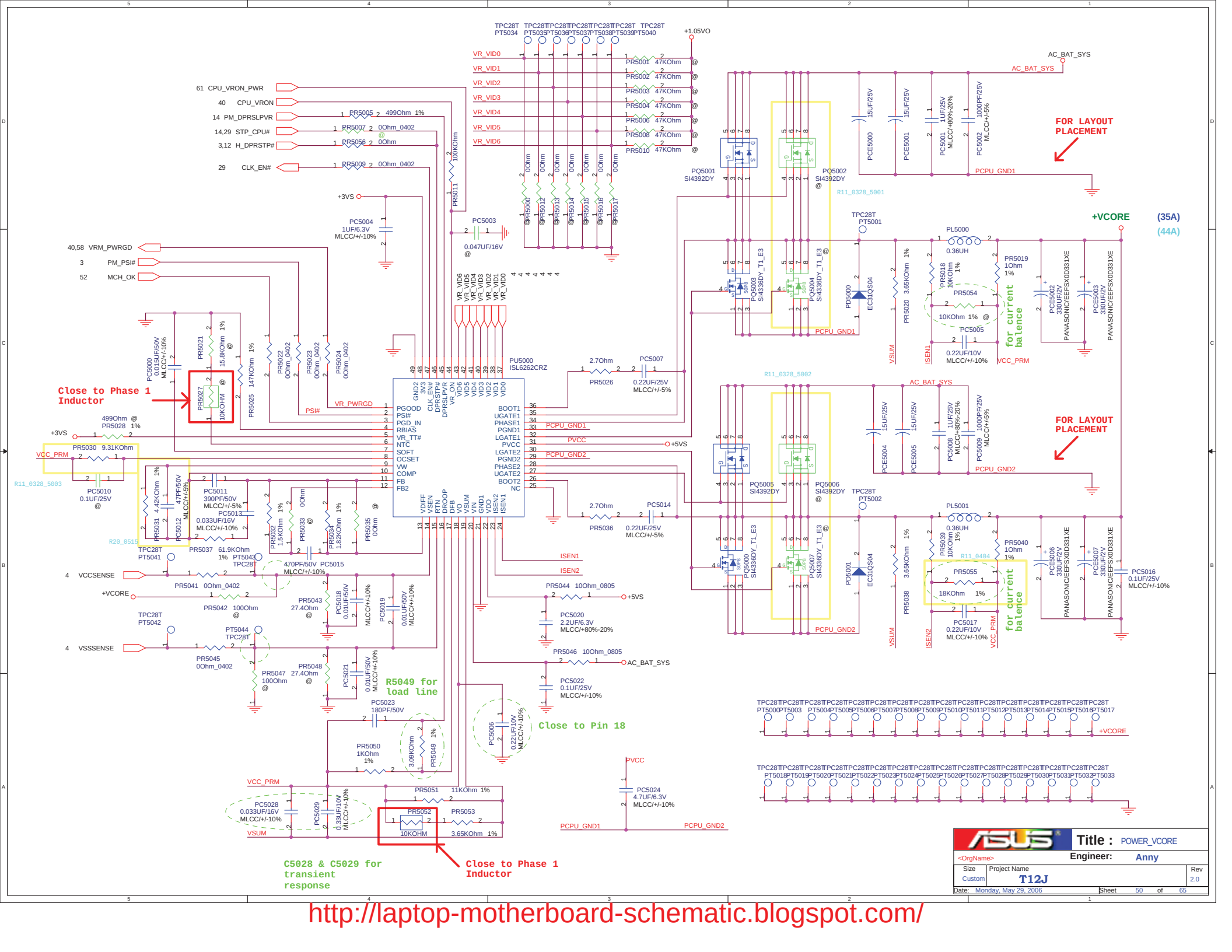
BLUETOOTH

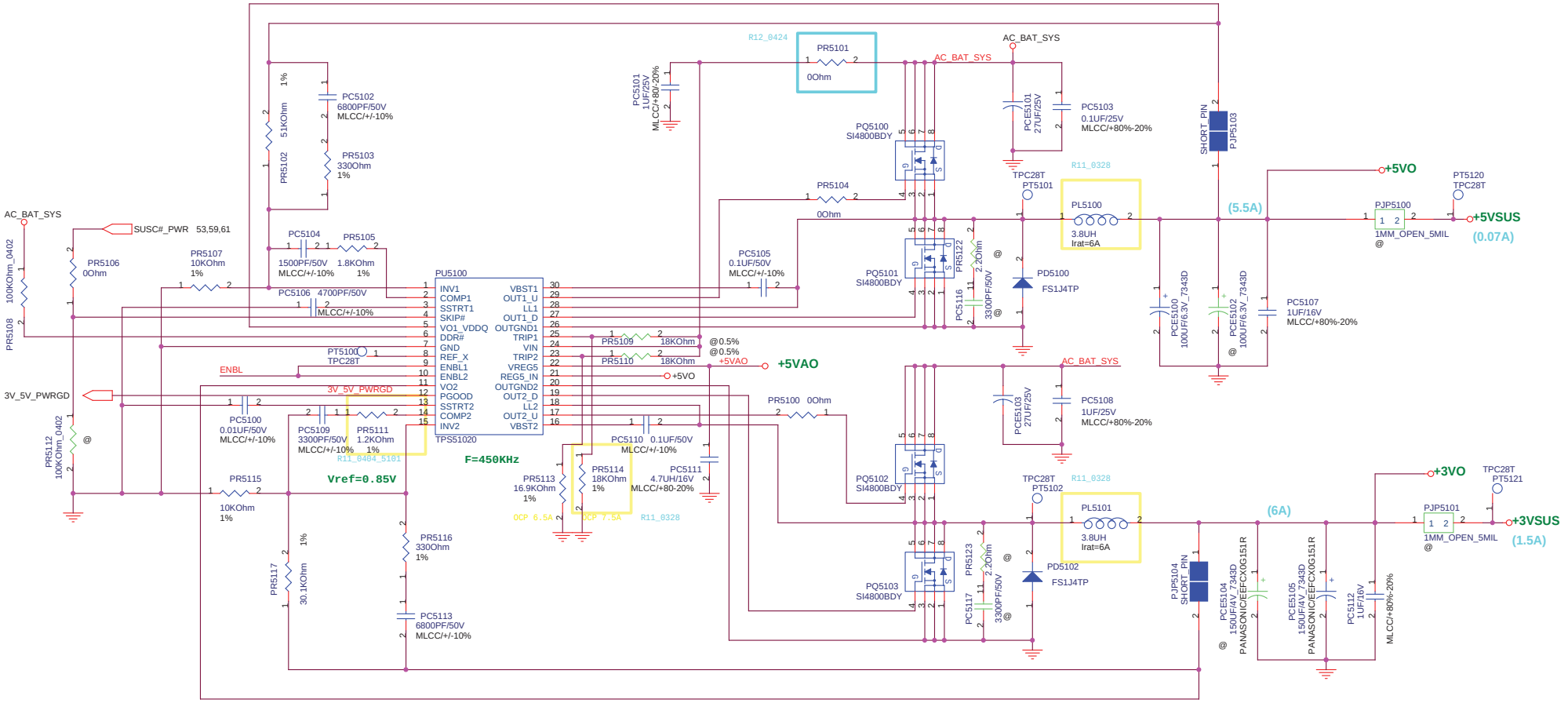


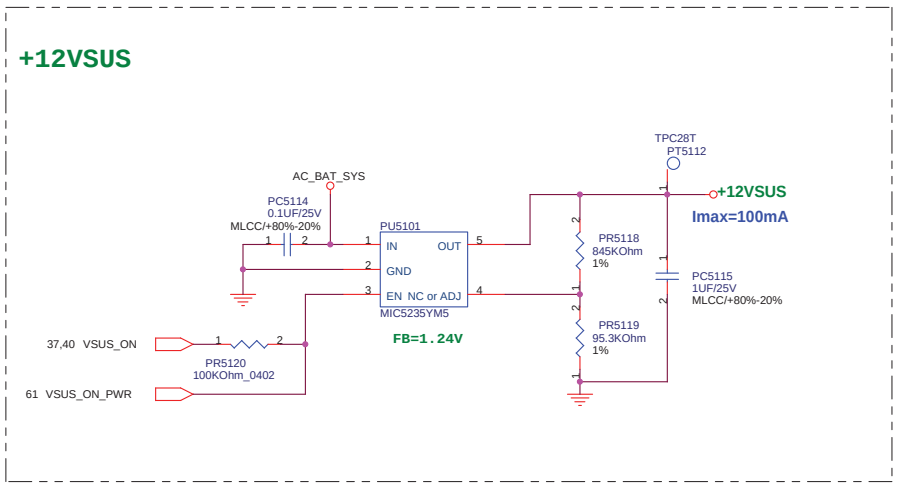
WLAN/BT ON/OFF Control

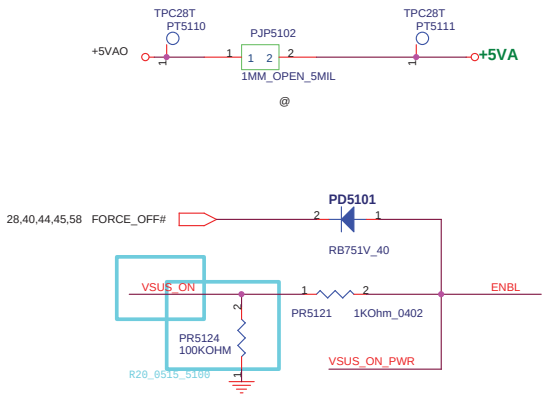


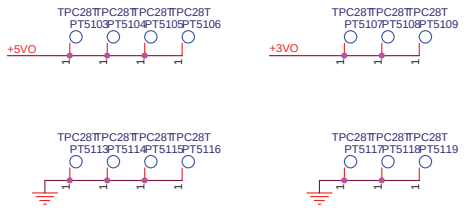
ASUSTek COMPUTER INC NPI	Title : BLUETOOTH&TPM	
	Engineer: Arthur & Bruce Chen	
Size: Custom	Project Name: T12J	Rev: 0.1
	P/N: <OrgAddr2>	
Date: Monday, May 29, 2006	Sheet 49 of 65	



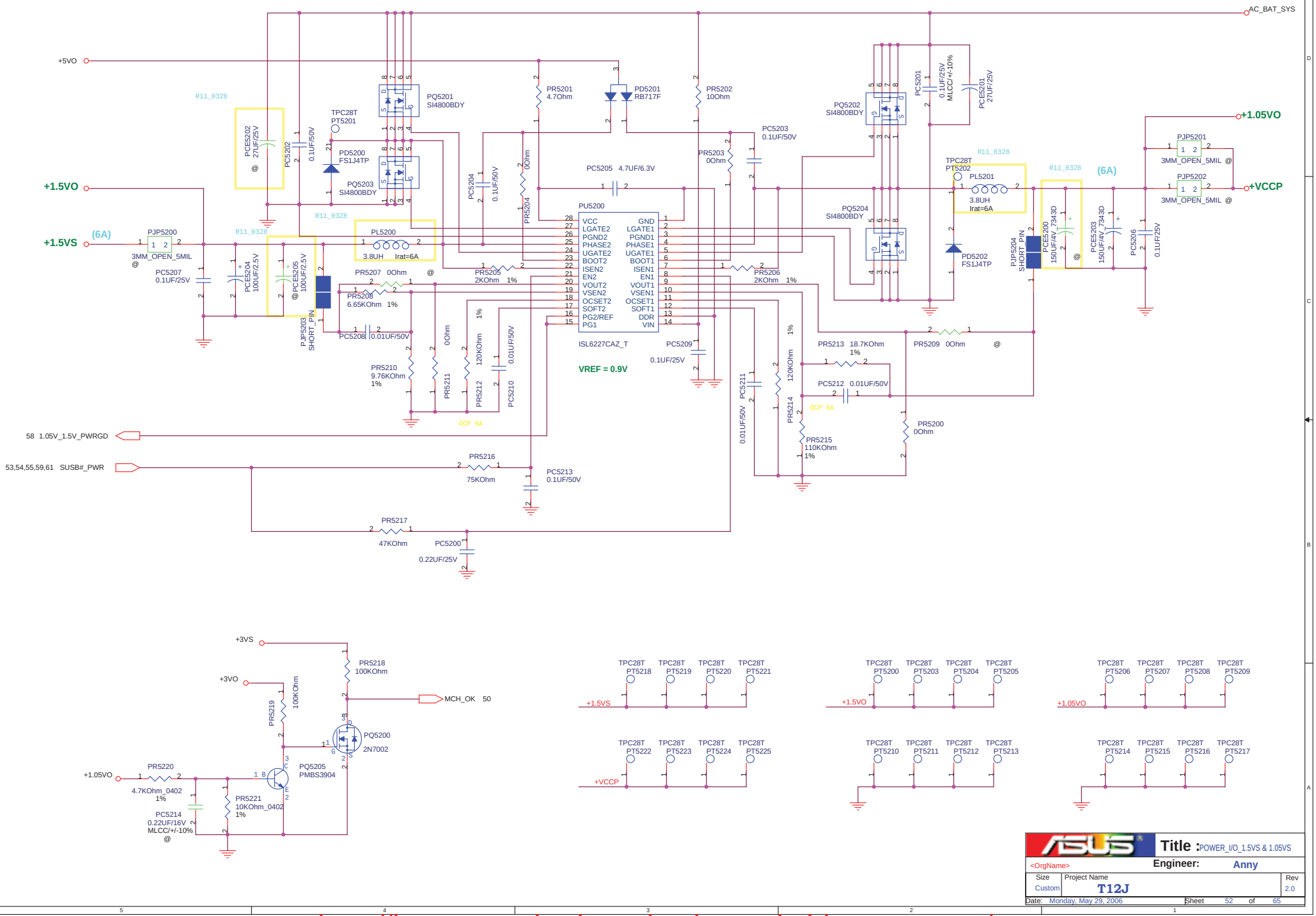


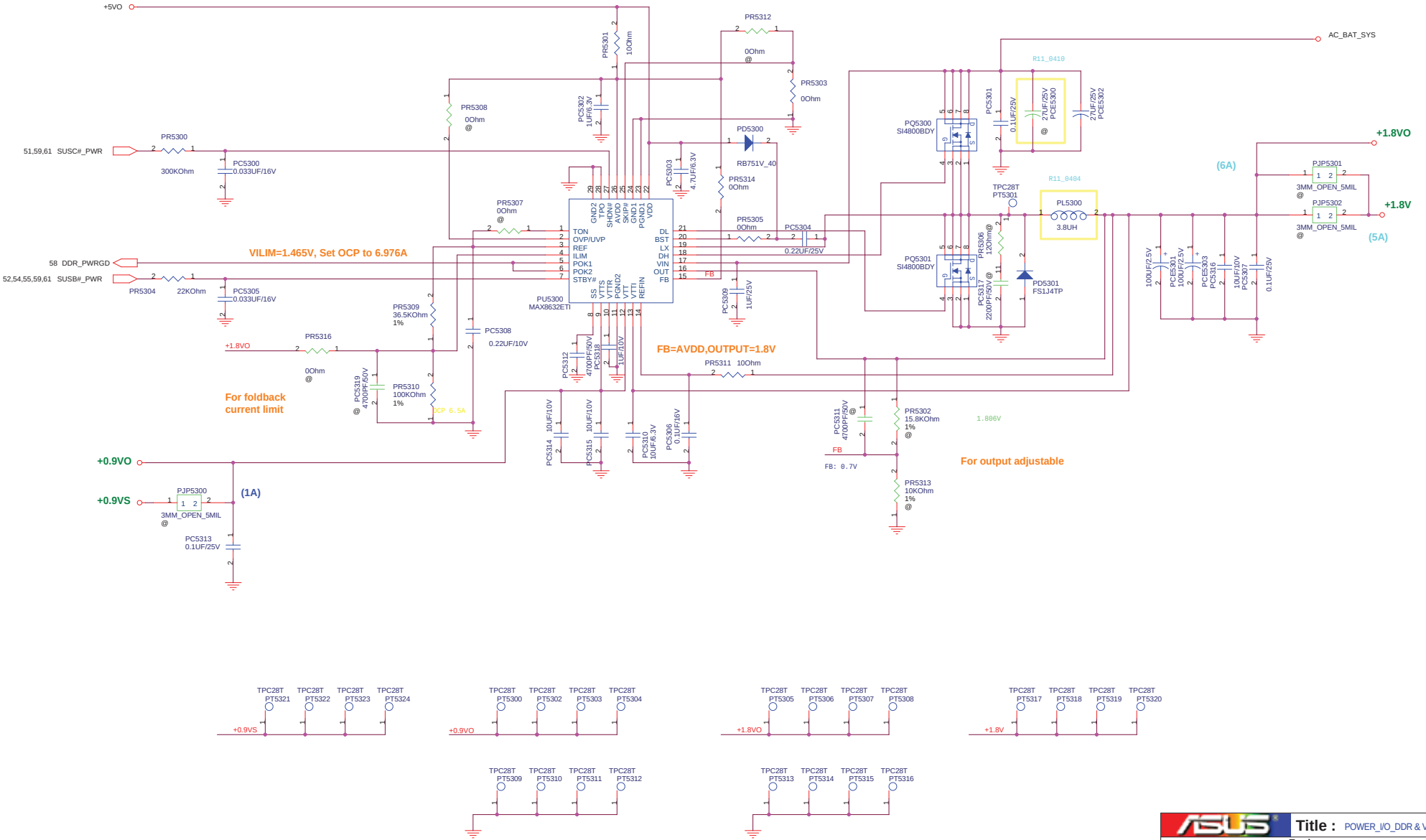




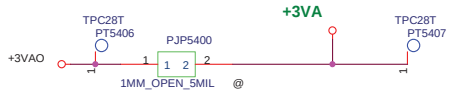


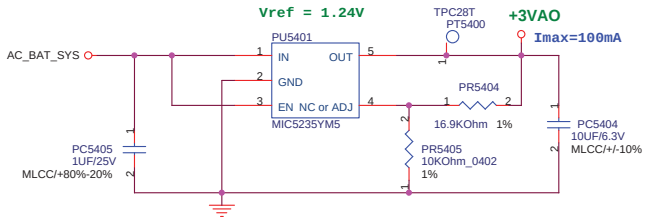
Title : POWER_SYSTEM		
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 51 of 65	



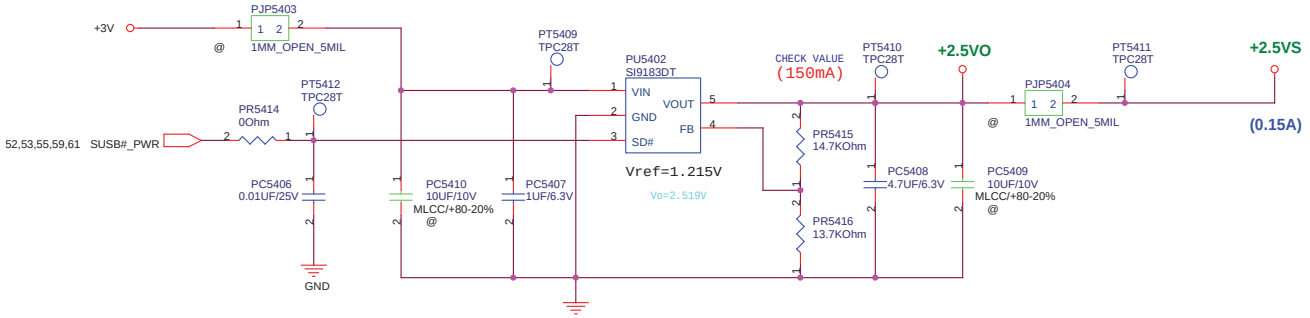


+3VA0

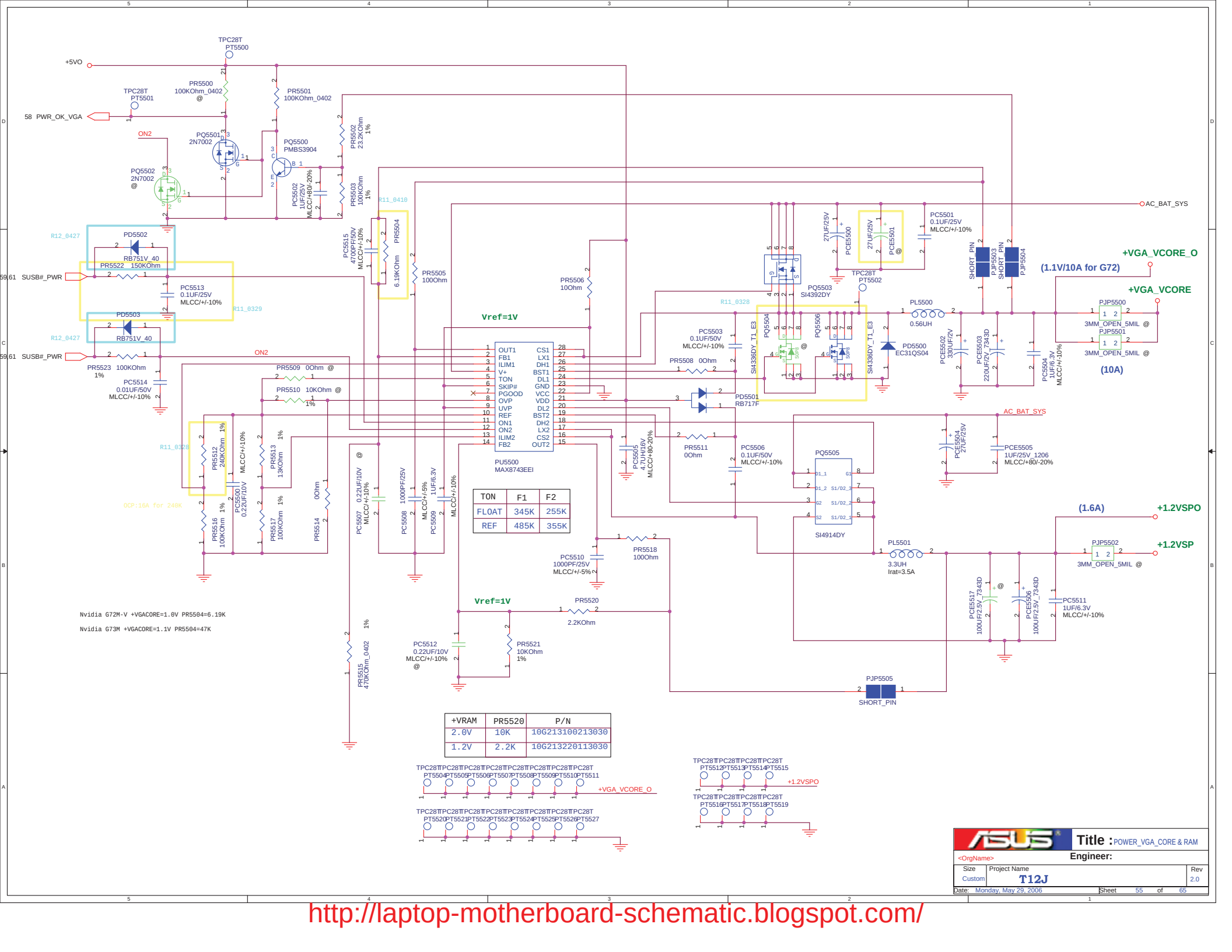




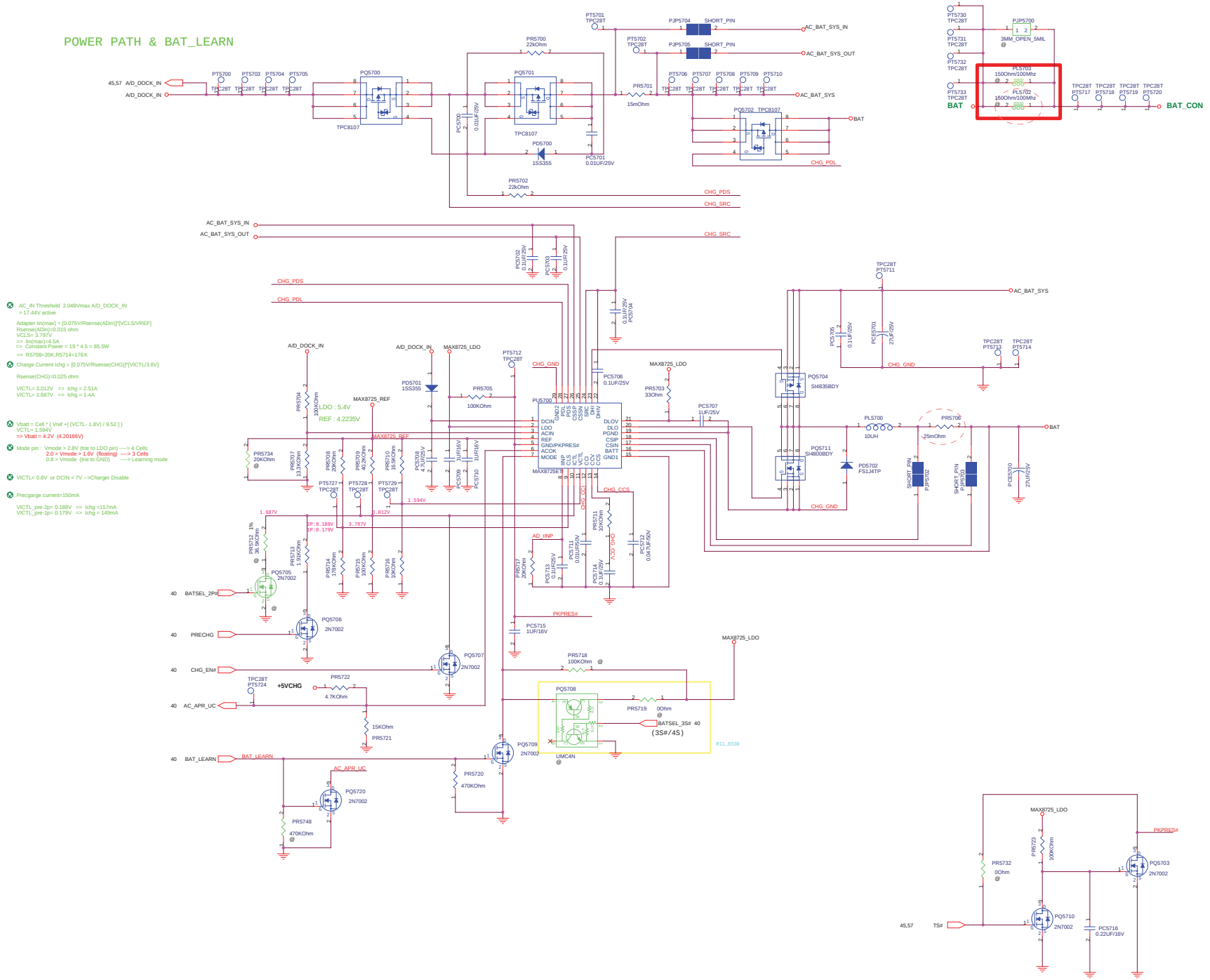
+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 54 of 65	

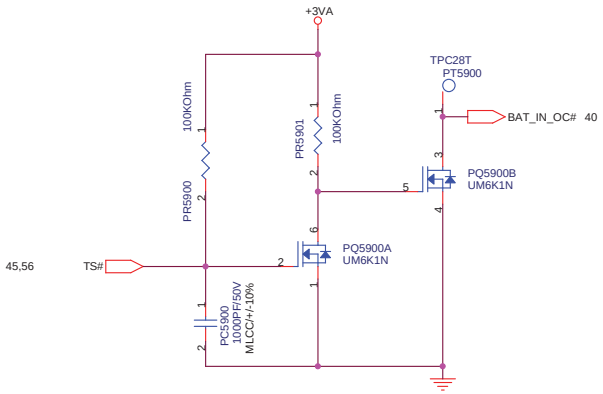


POWER PATH & BAT_LEARN

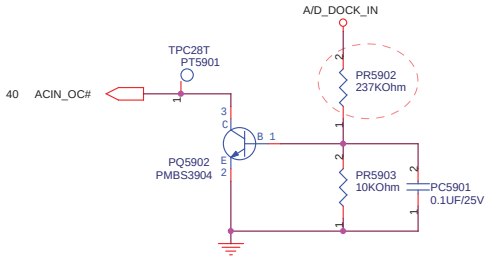


Title : POWER_CHARGER			
Engineer: Anny			
Size: Custom	Project Name: T12J		Rev: 2.0
Date: Monday, May 29, 2006	Sheet 56 of 65		

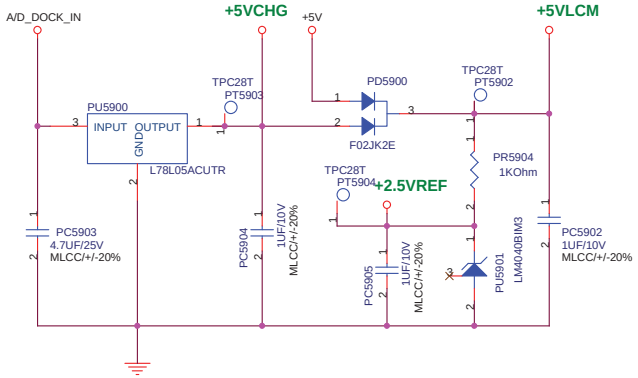
BATTERY IN DETECT



ADAPTER IN DETECT

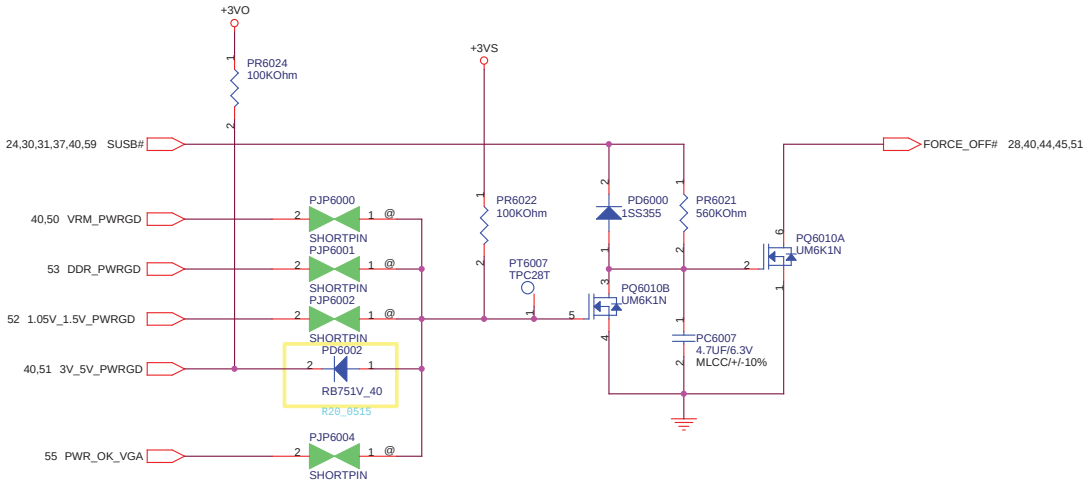


+5VLCM, +5VCHG & +2.5VREF



ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 57 of 65	

POWER GOOD DETECTER



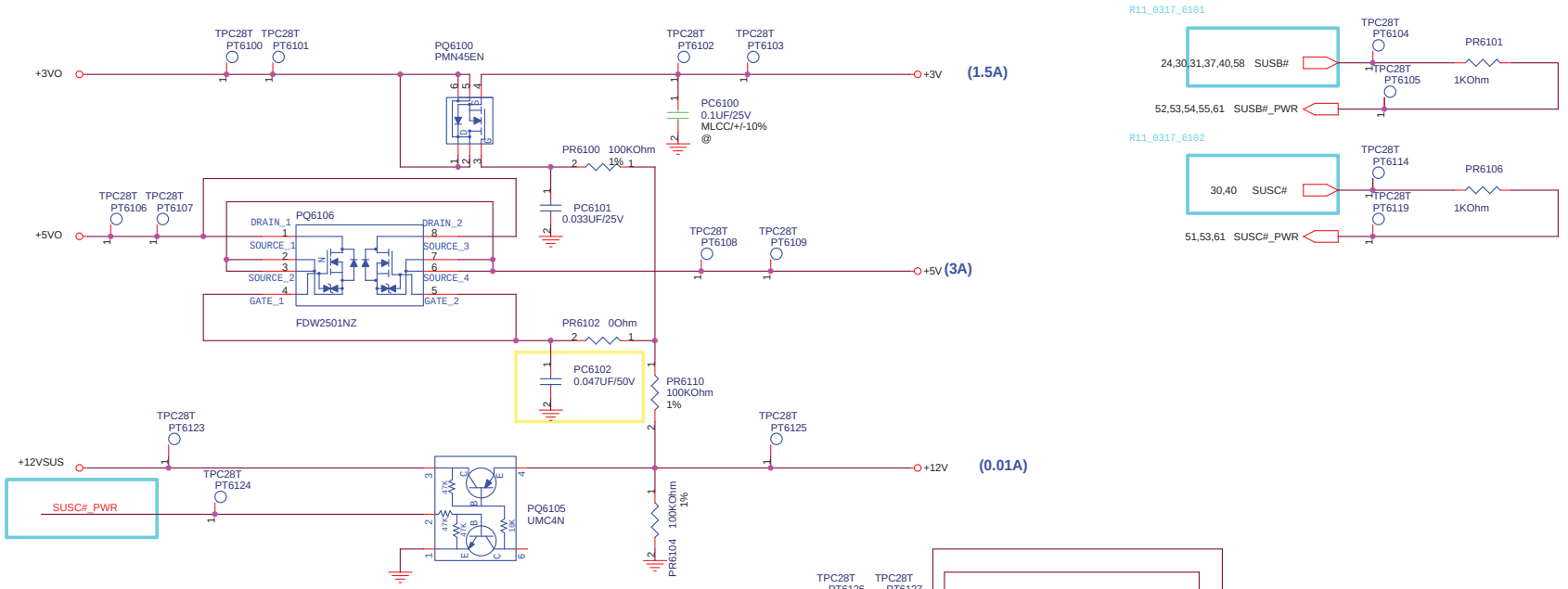
TPC28T PT6003 1 VRM_PWRGD
TPC28T PT6004 1 DDR_PWRGD
TPC28T PT6005 1 3V_5V_PWRGD
TPC28T PT6006 1 1.05V_1.5V_PWRGD
TPC28T PT6008 1 PWR_OK_VGA

R12_0424

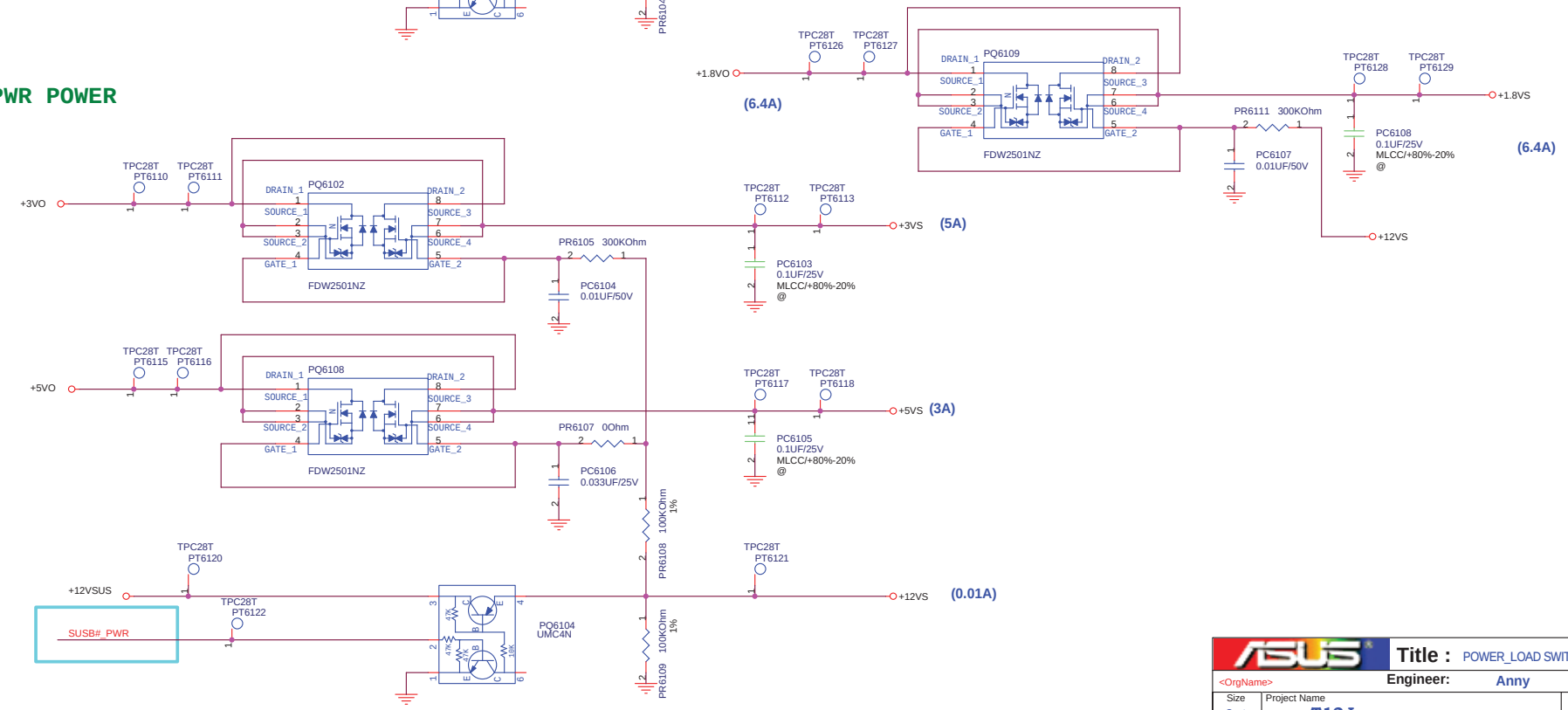
ASUS	Title : POWER_PROTECT	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 58 of 65	

(6.5A)

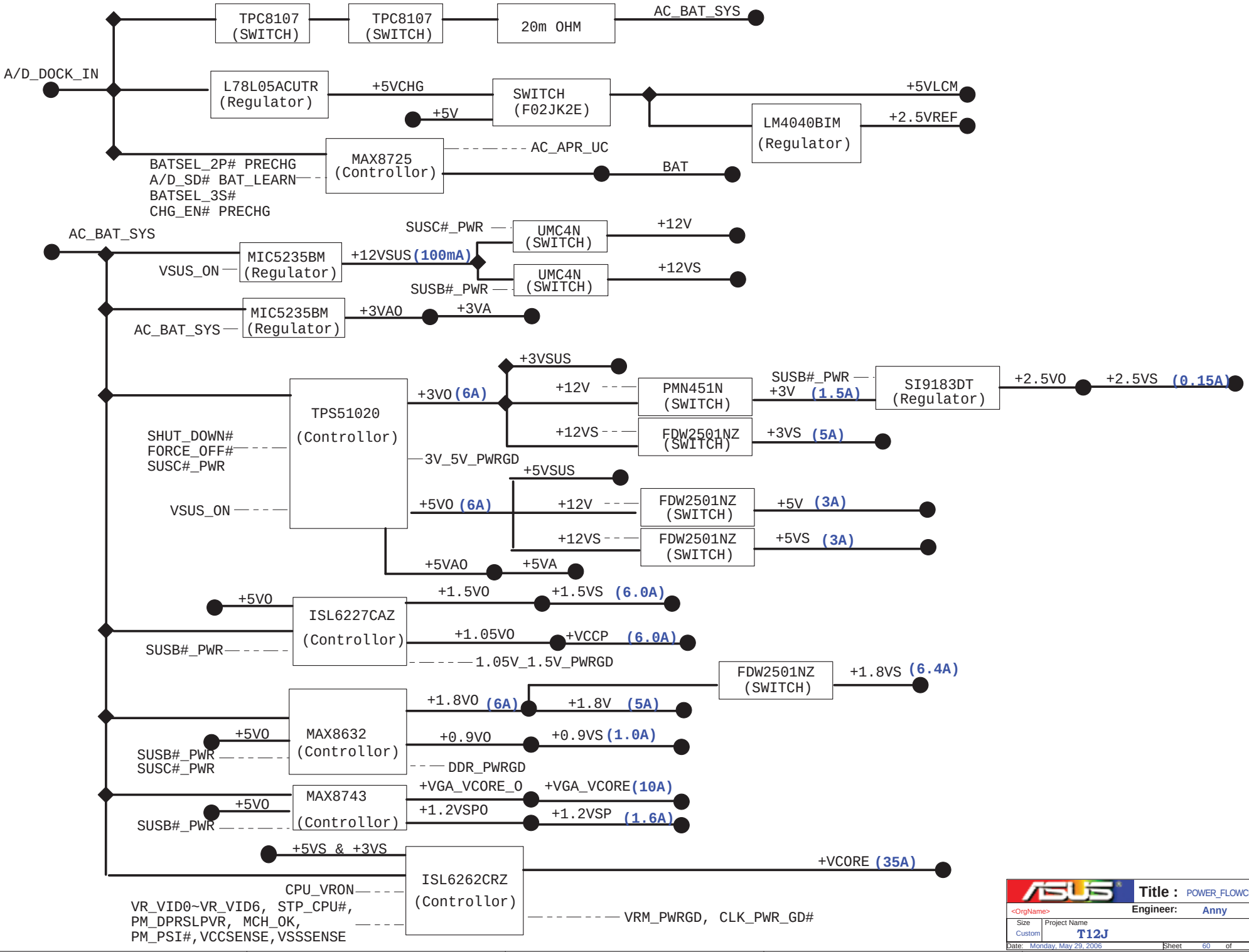
SUSC#_PWR POWER



SUSB#_PWR POWER



ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 59 of 65	



ASUS	Title :	POWER_FLOWCHART
<OrgName>	Engineer:	Anny
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 60 of 65	

AC_BAT_SYS — AC_BAT_SYS 24,45,50,51,52,53,54,55,56

+3VA — +3VA 12,24,28,30,39,40,44,54,57

+5VA — +5VA 51

+5VO — +5VO 51,52,53,55,59

+3VO — +3VO 51,52,58,59

+3VSUS — +3VSUS 13,14,15,31,37,51

+5VSUS — +5VSUS 15,44,51

+3V — +3V 30,32,33,44,49,54,59

+3VS — +3VS 6,10,13,14,15,16,17,19,21,22,24,25,26,27,28,29,30,33,34,35,36,37,38,39,40,46,47,49,50,52,58,59

+12VSUS — +12VSUS 51,59

+12V — +12V 30,42,59

+12VS — +12VS 24,36,39,49,59

+5V — +5V 24,30,42,44,57,59

+5VS — +5VS 14,15,25,28,30,38,39,40,44,47,50,59

+2.5VO — +2.5VO 54

+2.5VS — +2.5VS 10,21,26,30,54

+1.8VO — +1.8VO 53,59

+1.8V — +1.8V 6,9,16,17,30,53

+VCCP — +VCCP 4,5,7,9,10,12,15,30,52

+VCCP_AGTL+ — +VCCP_AGTL+ 3,4

+VCCP_GMCH — +VCCP_GMCH

+VCCP_ICH — +VCCP_ICH

+0.9VS — +0.9VS 18,23,30,53

BAT — BAT 56

+5VCHG — +5VCHG 56,57

+5VLCM — +5VLCM 57

+2.5VREF — +2.5VREF 57

+VCORE — +VCORE 4,28,50

BAT_CON — BAT_CON 45,56

FOR POWER TEST

+3VA

PJP6300 — SGL_JUMP @ — 1 — 1 2 — 2 — CPU_VRON_PWR 50

PJP6301 — SGL_JUMP @ — 1 — 1 2 — 2 — SUSB#_PWR — SUSB#_PWR 52,53,54,55,59

PJP6302 — SGL_JUMP @ — 1 — 1 2 — 2 — SUSC#_PWR — SUSC#_PWR 51,53,59

PJP6303 — SGL_JUMP @ — 1 — 1 2 — 2 — VSUS_ON_PWR — VSUS_ON_PWR 51

ASUS	Title : POWER_SIGNAL	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: T12J	Rev: 2.0
Date: Monday, May 29, 2006	Sheet 61 of 65	

Rev	Date	Description
1.0	10/04/05	1. Initial release.
1.1	12/26/05	

Rev	Date	Description

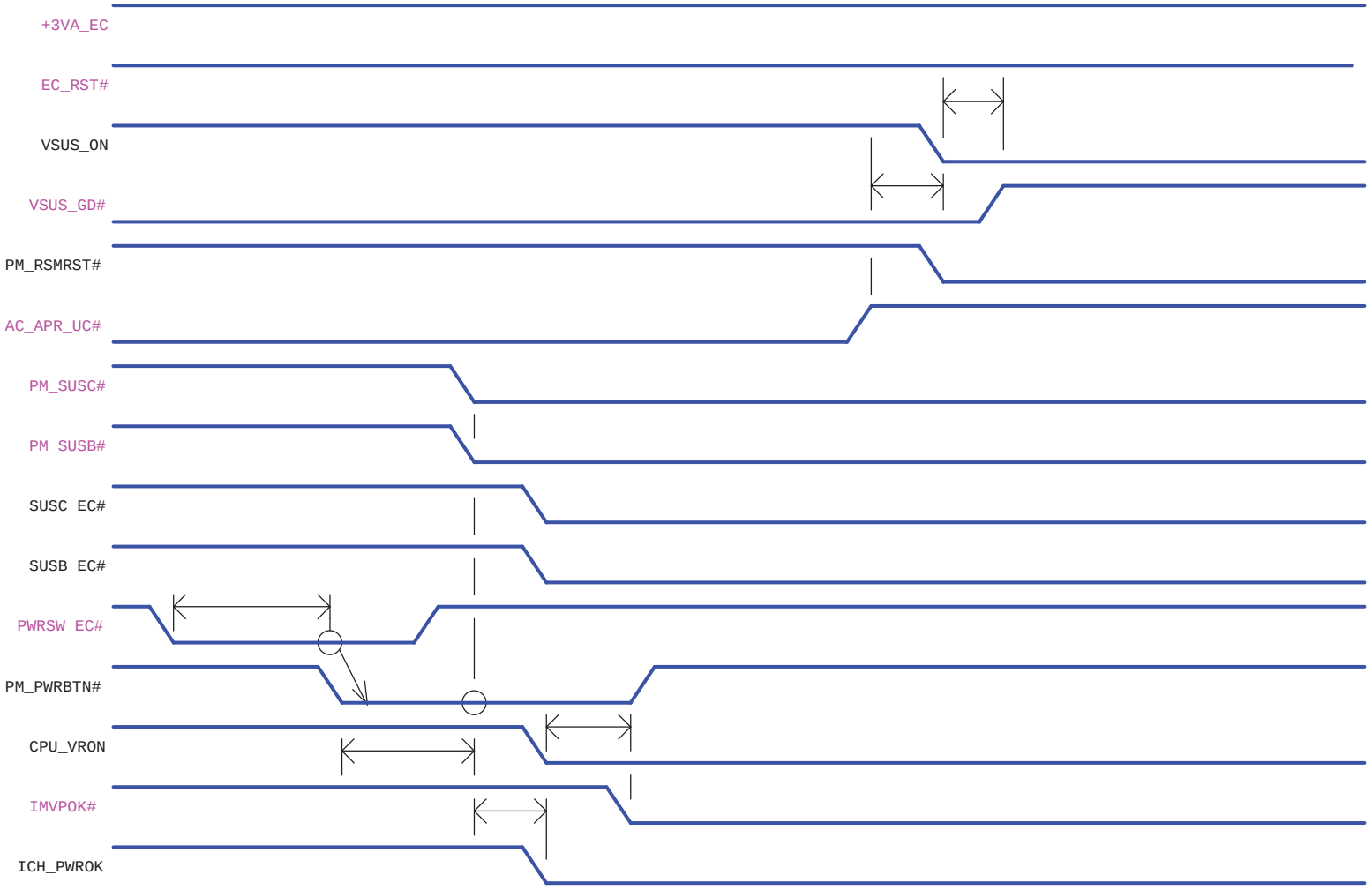
ASUSTek COMPUTER INC NPI

Title : History

Engineer: *Arthur & Bruce Chen*

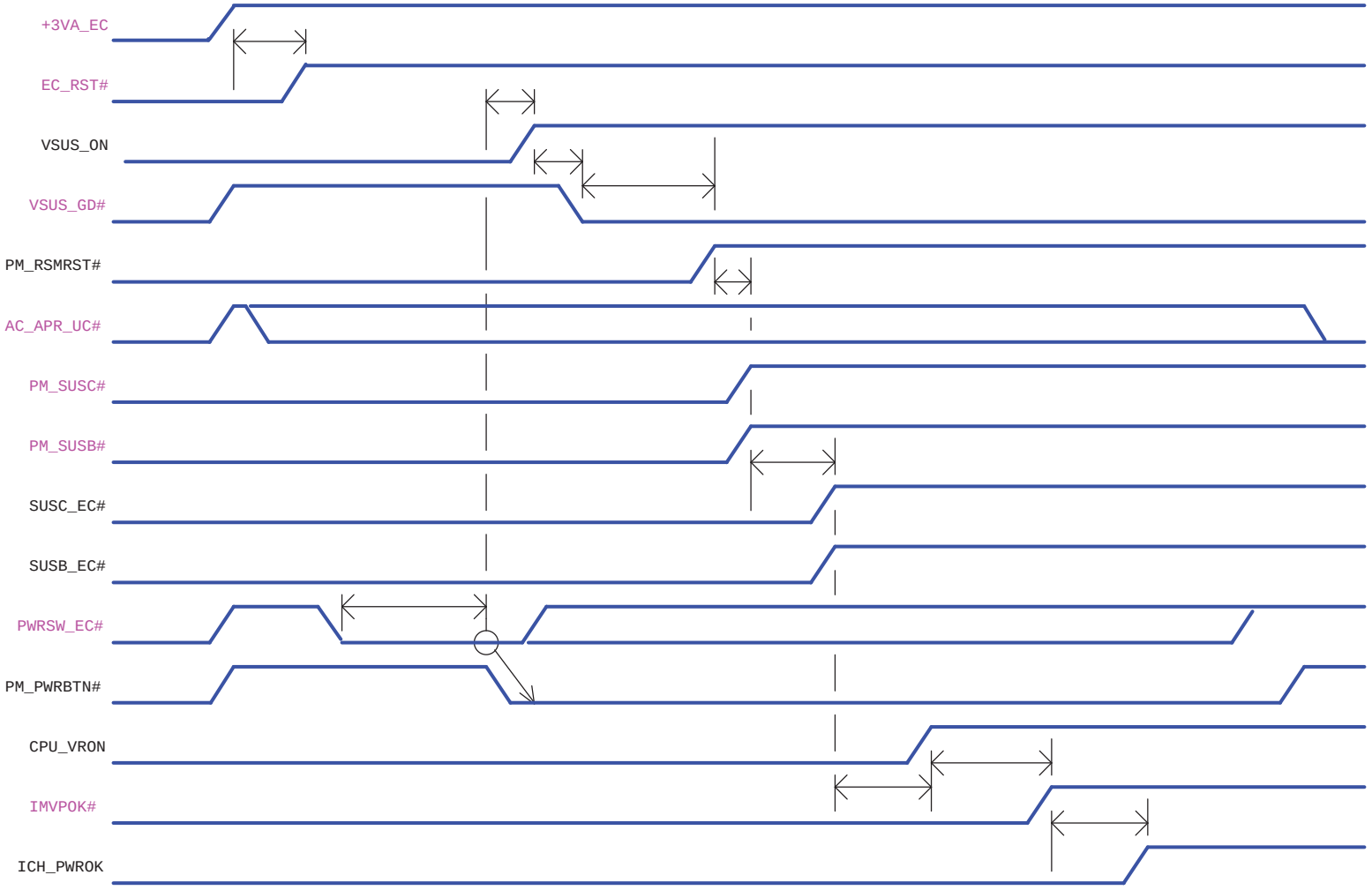
Size	Project Name	Rev
Custom	T12J	0.1
	P/N <OrgAddr2>	

Date: Monday, May 29, 2006 Sheet 62 of 65



POWER OFF TIMING

ASUSTek COMPUTER INC NPI	Title : Power OFF		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J		Rev: 0.1
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 63 of 65		



POWER ON TIMING

ASUSTek COMPUTER INC NPI	Title : Power ON		
	Engineer: Arthur & Bruce Chen		
Size: Custom	Project Name: T12J		Rev: 0.1
	P/N: <OrgAddr2>		
Date: Monday, May 29, 2006	Sheet 64 of 65		

R1.0

Item	Before	After	Reason	Owner	Date

R1.1

Item	Before	After	Reason	Owner	Date
R11_0317_6001	Pull hi to +5VA	Pull hi to +3VA	To meet EC power request		2006.03.17
R11_0317_5401	IC:CM8562GISTR	IC:SI9183DT	Cost down		2006.03.17
R11_0317_6101	SUSB_ON	SUSB#	For EE request		2006.03.17
R11_0317_6102	SUSC_ON	SUSC#	For EE request		2006.03.17
R11_0317_5701	PD5705: 1SS355(07G001007100)	PD5705: RB751V_40(07G004020710)	Down Vf		2006.03.17
R11_0322_5702	Error fumction	Del Error fumction and add PD5707			2006.03.22
R11_0328_5001 ~ R11_0328_5003	mount: PQ5002, PQ5004, PQ5006, PQ5007 PR5030 16K	unmount: PQ5002, PQ5004, PQ5006, PQ5007 PR5030 change to 9.31K to tune OCP to 47A	Cost down		2006.03.28
R11_0404_5101	2.7K	1.2K	避免磁場干擾		2006.03.28
R12_0413_57	AD error and pwr limit function	DEL AD error and pwr limit function	Cost down		2006.04.24
R12_0413_60	batteru OVP protect function	DEL batteru OVP protect function	Cost down		2006.04.24
R12_0427		Add PD5502 and PD5503	Add PD5502 and PD5503 to avoid on1 voltage drop slow when disable.		

R2.0

Item	Before	After	Reason	Owner	Date
R20_0515_5100		add PR5124	Pull ground to avoid vsus_on is float.		2006.05.15

ASUS

Title : POWER_PIC

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	NAPA	2.0

Date: Monday, May 29, 2006 Sheet 65 of 65